Chapter 8. Field Effect Transistor

Field Effect Transistor:

The field effect transistor is a semiconductor device, which depends for its operation on the control of current by an electric field. There are two of field effect transistors:

1. JFET (Junction Field Effect Transistor)
2. MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

The FET has several advantages over conventional transistor.

1. In a conventional transistor, the operation depends upon the flow of majority and minority carriers. That is why it is called bipolar transistor. In FET the operation depends upon the flow of majority carriers only. It is called unipolar device.
2. The input to conventional transistor amplifier involves a forward biased PN junction with its inherently low dynamic impedance. The input to FET involves a reverse biased PN junction hence the high input impedance of the order of M-ohm.
3. It is less noisy than a bipolar transistor.
4. It exhibits no offset voltage at zero drain current.
5. It has thermal stability.
6. It is relatively immune to radiation.

The main disadvantage is its relatively small gain bandwidth product in comparison with conventional transistor.

Operation of FET:

Consider a sample bar of N-type semiconductor. This is called N-channel and it is electrically equivalent to a resistance as shown in **fig. 1**.

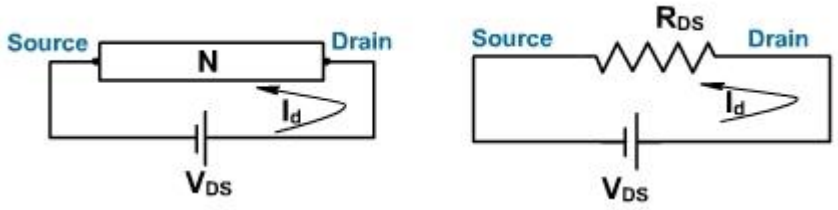


Fig. 1

Ohmic contacts are then added on each side of the channel to bring the external connection. Thus if a voltage is applied across the bar, the current flows through the channel.

The terminal from where the majority carriers (electrons) enter the channel is called source designated by S. The terminal through which majority carriers leaves the channel is called drain and designated by D. For an N-channel device, electrons are the majority carriers. Hence the circuit behaves like a dc voltage V_{DS} applied across a resistance R_{DS}. The resulting current is the drain current I_D. If V_{DS} increases, I_D increases proportionally.

Now on both sides of the n-type bar heavily doped regions of p-type impurity have been formed by any method for creating pn junction. These impurity regions are called gates (gate1 and gate2) as shown in **fig. 2**.

Both the gates are internally connected and they are grounded yielding zero gate source voltage (V_{GS} =0). The word gate is used because the potential applied between gate and source controls the channel width and hence the current.

As with all PN junctions, a depletion region is formed on the two sides of the reverse biased PN junction. The current carriers have diffused across the junction, leaving only uncovered positive ions on the n side and negative ions on the p side. The depletion region width increases with the magnitude of reverse bias. The

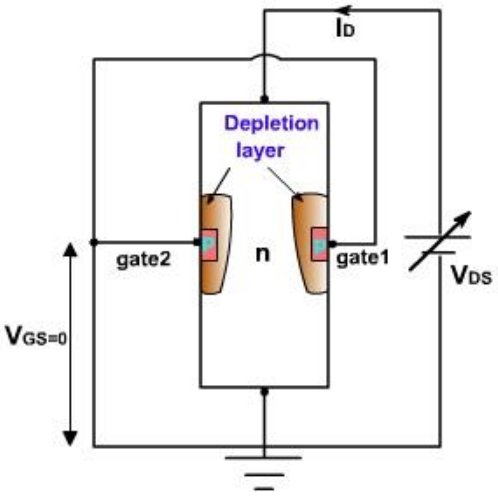


Fig. 2

conductivity of this channel is normally zero because of the unavailability of current carriers.

The potential at any point along the channel depends on the distance of that point from the drain, points close to the drain are at a higher positive potential, relative to ground, then points close to the source. Both depletion regions are therefore subject to greater reverse voltage near the drain. Therefore the depletion region width increases as we move towards drain. The flow of electrons from source to drain is now restricted to the narrow channel between the no conducting depletion regions. The width of this channel determines the resistance between drain and source.

consider now the behavior of drain current I_D vs drain source voltage V_{DS}. The gate source voltage is zero therefore V_{GS}= 0. Suppose that V_{DS} is gradually linearly increased linearly from 0V. I_D also increases.

Since the channel behaves as a semiconductor resistance, therefore it follows ohm's law. The region is called ohmic region, with increasing current, the ohmic voltage drop between the source and the channel region reverse biased the junction, the conducting portion of the channel begins to constrict and I_D begins to level off until a specific value of V_{DS} is reached, called the **pinch of voltage V_P**.

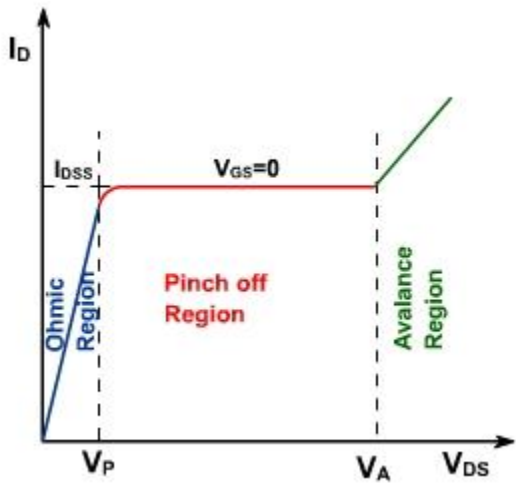


Fig. 3

At this point further increase in V_{DS} do not produce corresponding increase in I_D. Instead, as V_{DS}increases, both depletion regions extend further

into the channel, resulting in a no more cross section, and hence a higher channel resistance. Thus even though, there is more voltage, the resistance is also greater and the current remains relatively constant. This is called pinch off or saturation region. The current in this region is maximum current that FET can produce and designated by I_{DSS}. (Drain to source current with gate shorted).

As with all pn junctions, when the reverse voltage exceeds a certain level, avalanche breakdown of pn junction occurs and I_D rises very rapidly as shown in **fig. 3**.

Consider now an N-channel JFET with a reverse gate source voltage as shown in **fig. 4**.

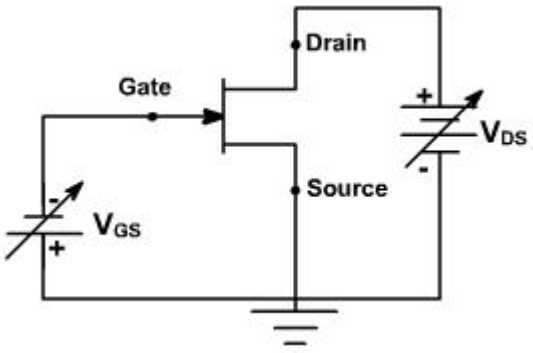


Fig. 4

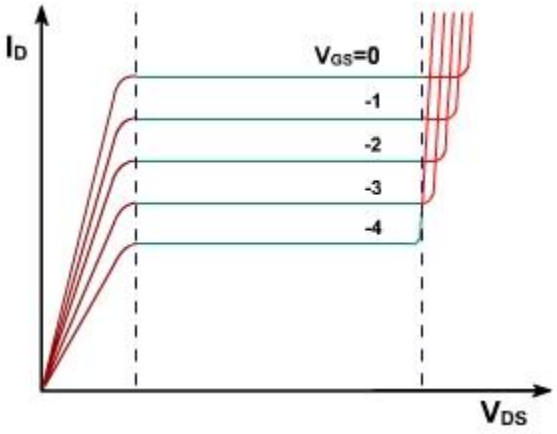


Fig. 5

The additional reverse bias, pinch off will occur for smaller values of $|V_{DS}|$, and the maximum drain current will be smaller. A family of curves for different values of V_{GS}(negative) is shown in **fig. 5**.

Suppose that V_{GS}= 0 and that due of V_{DS} at a specific point along the channel is +5V with respect to ground. Therefore reverse voltage across either p-n junction is now 5V. If V_{GS} is

decreased from 0 to −1V the net reverse bias near the point is 5 - (-1) = 6V. Thus for any fixed value of V_{DS}, the channel width decreases as V_{GS} is made more negative.

Thus I_D value changes correspondingly. When the gate voltage is negative enough, the depletion layers touch each other and the conducting channel pinches off (disappears). In this case the drain current is cut off. The gate voltage that produces cut off is symbolized $V_{GS}(off)$. It is same as pinch off voltage.

Since the gate source junction is a reverse biased silicon diode, only a very small reverse current flows through it. Ideally gate current is zero. As a result, all the free electrons from the source go to the drain i.e. $I_D = I_S$. Because the gate draws almost negligible reverse current the input resistance is very high 10's or 100's of M ohm. Therefore where high input impedance is required, JFET is preferred over BJT. The disadvantage is less control over output current i.e. FET takes larger changes in input voltage to produce changes in output current. For this reason, JFET has less voltage gain than a bipolar amplifier.

Biasing the Field Effect Transistor

Transductance Curves:

The transductance curve of a JFET is a graph of output current (I_D) vs input voltage (V_{GS}) as shown in **fig. 1**.

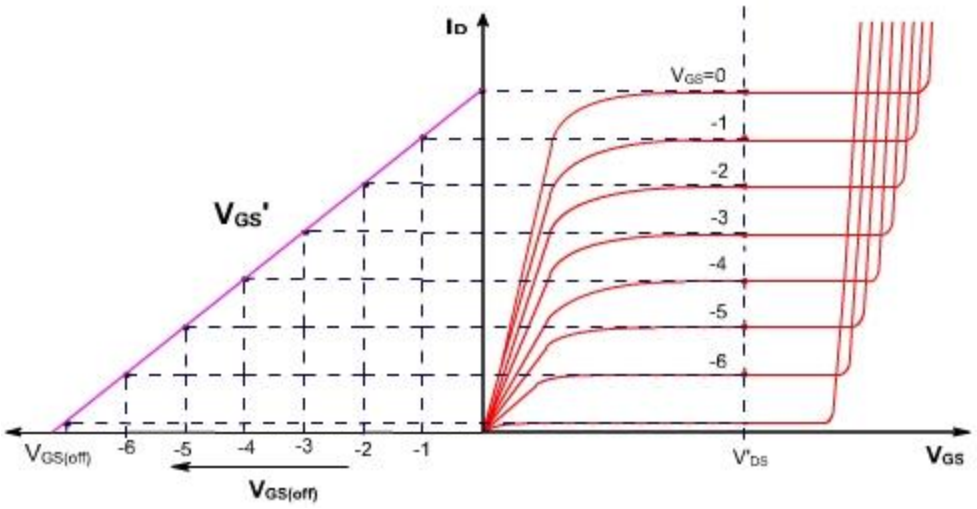


Fig. 1

By reading the value of I_D and V_{GS} for a particular value of V_{DS}, the transductance curve can be plotted. The transductance curve is a part of parabola. It has an equation of

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(Off)}}\right)^2$$

Data sheet provides only I_{DSS} and V_{GS}(off) value. Using these values the transductance curve can be plotted.

Biasing the FET:

The FET can be biased as an amplifier. Consider the common source drain characteristic of a JFET. For linear amplification, Q point must be selected somewhere in the saturation region. Q point is selected on the basis of ac performance i.e. gain, frequency response, noise, power, current and voltage ratings.

Gate Bias:

Fig. 2, shows a simple gate bias circuit.

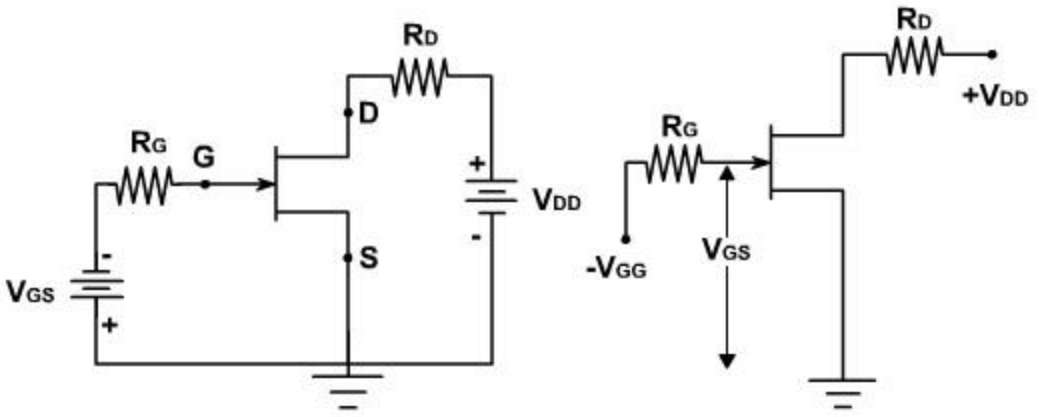


Fig. 2

Separate V_{GS} supply is used to set up Q point. This is the worst way to select Q point. The reason is that there is considerable variation between the maximum and minimum values of FET parameters e.g.

	I_{DSS}	V_{GS}(off)
Minimum	4mA	-2V
Maximum	13mA	-8V

This implies that the minimum and maximum transductance curves are displaced as shown in **fig. 3**.

Gate bias applies a fixed voltage to the gate. This fixed voltage results in a Q point that is highly sensitive to the particular JFET used. For instance, if V_{GS}= -1V the Q point may very from Q_1 to Q_2 depending upon the JFET parameter is use.

At Q_1, I_D= 0.016 (1 - (1/8))^2 = 12.3 mA

At Q_2, I_D= 0.004 (1-(1/2))^2 = 1 mA.

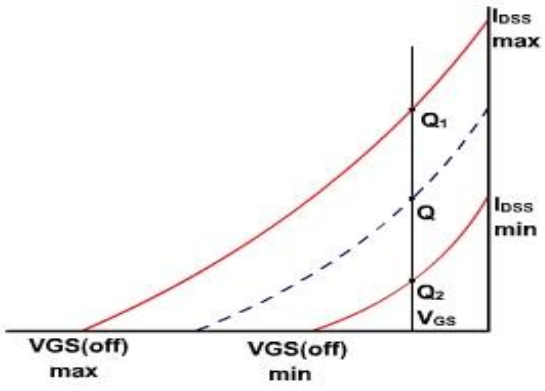


Fig. 3

The variation in drain current is very large.

Self Bias:

Fig. 4, shows a self bias circuit another way to bias a FET. Only a drain supply is used and no gate supply. The idea is to use the voltage across R_S to produce the gate source reverse voltage.

This is a form of a local feedback similar to that used with bipolar transistors. If drain current increases, the voltage drop across R_S increases because the I_D R_S increases. This increases the gate source reverse voltage which makes the channel narrow and reduces the drain current. The overall effect is to partially offset the original increase in drain current. Similarly, if I_D decreases, drop across R_S decreases, hence reverse bias decreases and I_D increases.

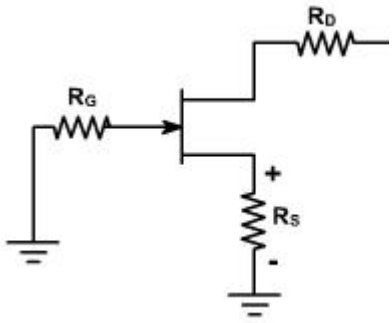


Fig. 4

Since the gate source junction is reverse biased, negligible gate current flows through R_G and so the gate voltage with respect to ground is zero.

$V_G = 0$;

The source to ground voltage equals the product of the drain current and the source resistance.

$\backslash V_S = I_D R_S$.

The gate source voltage is the difference between the gate voltage and the source voltage.

$V_{GS} = V_G - V_S = 0 - I_D R_S$

$V_{GS} = -I_D R_S$.

This means that the gate source voltage equals the negative of the voltage across the source resistor. The greater the drain current, the more negative the gate source voltage becomes.

Rearranging the equation:

$I_D = -V_{GS} / R_S$

The graph of this equation is called self base line a shown in **Fig. 5**.

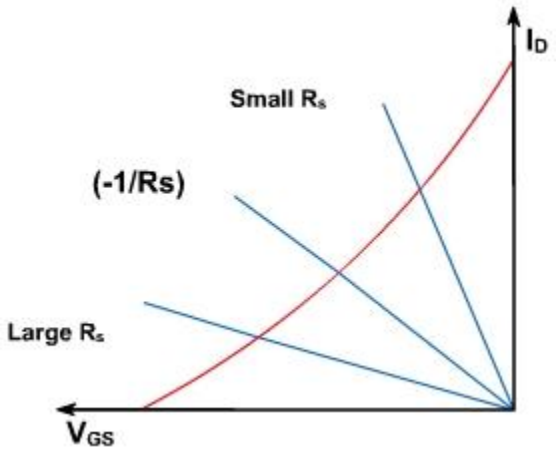


Fig. 5

The operating point on transductance curve is the intersection of self bias line and transductance curve. The slope of the line is $(-1 / R_S)$. If the source resistance is very large ($-1 / R_S$ is small) then Q-point is far down the transductance curve and the drain current is small. When R_S is small, the Q point is far up the transductance curve and the drain current is large. In between there is an optimum value of R_S that sets up a Q point near the middle of the transductance curve.

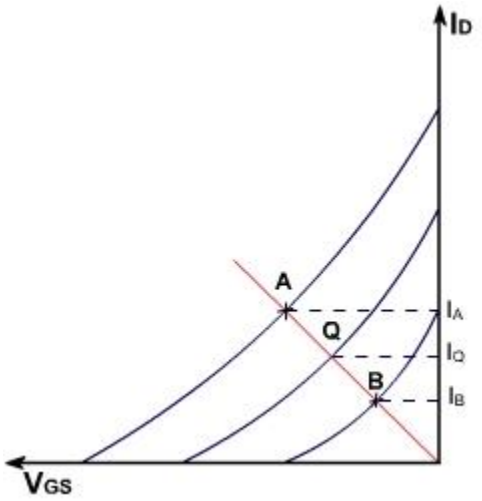


Fig. 6

The transductance curve varies widely for FET (because of variation in I_{DSS} and V_{GS}(off)) as shown in **fig. 6**. The

actual curve may be in between there extremes. A and B are the optimum points for the two extreme curves. To find the optimum resistance R_S, so that Q-point is correct for all the curves, A and B points are joined such that it passes through origin.

The slope of this line gives the resistance value R_S($V_{GS} = -I_D R_S$). The current I_Q is such that $I_A > I_Q > I_B$. Here A, Q and B all points are in straight line.

Consider the case where a line drawn to pass between points A and B does not pass through the origin. The equation $V_{GS} = - I_D R_S$ is not valid. The equation of this line is $V_{GS} = V_{GG}$ – $I_D R_S$.

Such a bias relationship may be obtained by adding a fixed bias to the gate in addition to the source self bias as shown in **fig. 7**.

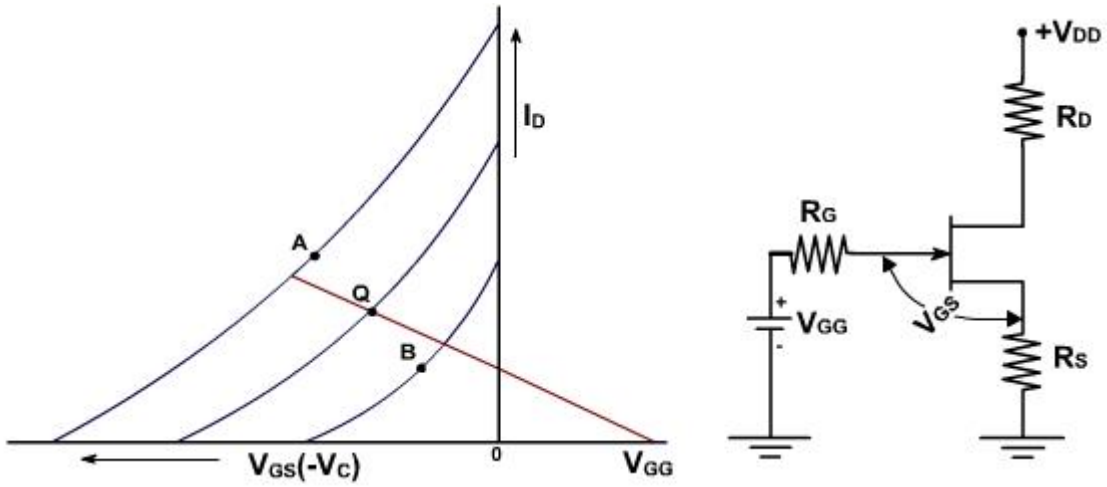


Fig. 7

In this circuit.

$V_{GG} = R_S I_G + V_{GS} + I_D R_S$

Since $R_S I_G = 0$;

$V_{GG} = V_{GS} + I_D R_S$

or $V_{GS} = V_{GG} - I_D R_S$

Voltage Divider Bias :

The biasing circuit based on single power supply is shown in **fig. 1**. This is similar to the voltage divider bias used with a bipolar transistor.

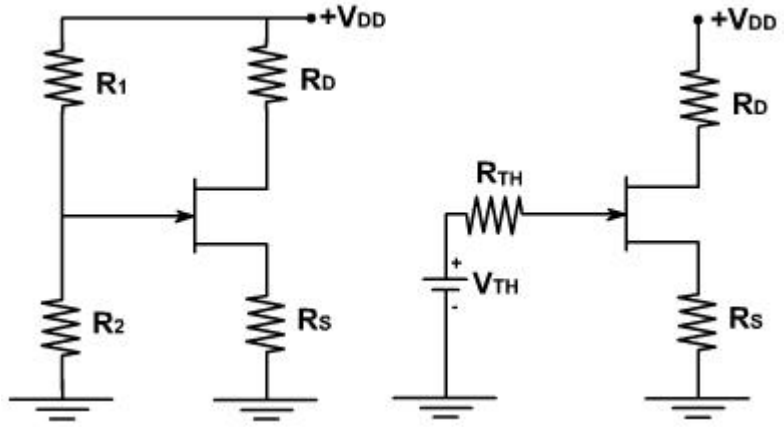


Fig. 1

The Thevenin voltage V_{TH} applied to the gate is

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{DD}$$

The Thevenin resistance is given as

$$R_{TH} = \frac{R_2 R_1}{R_1 + R_2}$$

The gate current is assumed to be negligible. V_{TH} is the dc voltage from gate to ground.

$$V_{TH} = V_{GS} + V_S \text{ (neglecting } I_G)$$
$$\therefore V_S = V_{TH} = V_{GS}$$

The drain current ID is given by

$$I_D = \frac{V_{TH} - V_{GS}}{R_S}$$

and the dc voltage from the drain to ground is $V_D = V_{DD}$ **&#65533;** $I_D R_D$.

If V_{TH} is large enough to swamp out V_{GS} the drain current is approximately constant for any JFET as shown in **fig. 2**.

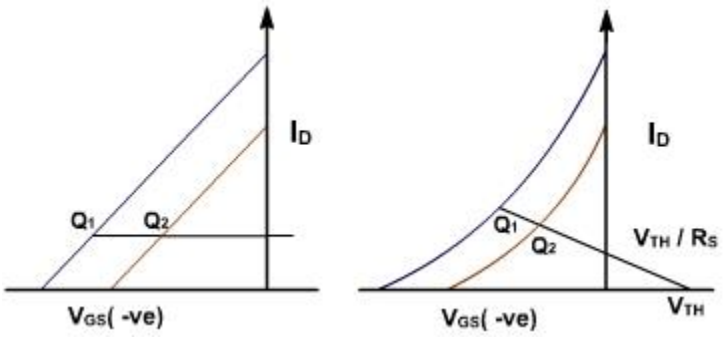


Fig. 2

There is a problem in JFET. In a BJT, V_{BE} is approximately 0.7V, with only minor variations from one transistor to other. In a FET, V_{GS} can vary several volts from one JFET to another. It is therefore, difficult to make V_{TH} large enough to swamp out V_{GS}. For this reason, voltage divider bias is less effective with, FET than BJT. Therefore, V_{GS} is not negligible. The current increases slightly from Q2 to Q1. However, voltage divider bias maintains I_D nearly constant.

Consider a voltage divider bias circuit shown in **fig. 3**.

$V_{GS(min)} = -1, \quad V_{GS(max)} = -5V$

$V_{TH} = 15V$

$$I_{D(min)} = \frac{15-(-1)}{7.5K} = 2.13 \text{ mA}$$

$$I_{D(max)} = \frac{15-(-5)}{7.5K} = 2.67 \text{ mA}$$

Difference in $I_{D\,(min)}$ and $I_{D\,(max)}$ is less

$V_{D\,(max)} = 30 - 2.13 * 4.7 = 20$ V

$V_{D\,(min)} = 30 - 2.67 * 4.7 = 17.5$ V

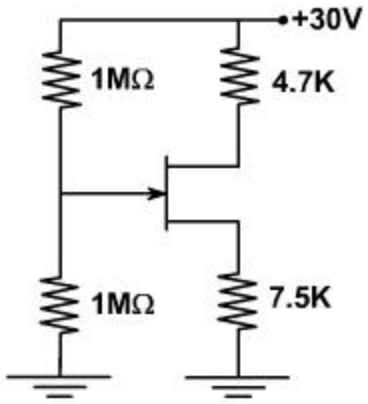


Fig. 3

Current Source Bias:

This is another way to produce solid Q point. The aim is to produce a drain current that is independent of V_{GS}. Voltage divider bias and self bias attempt to do this by swamping out of variations in V_{GS}.

Using two power supplies:

The current source bias can be used to make I_D constant **fig. 4**.

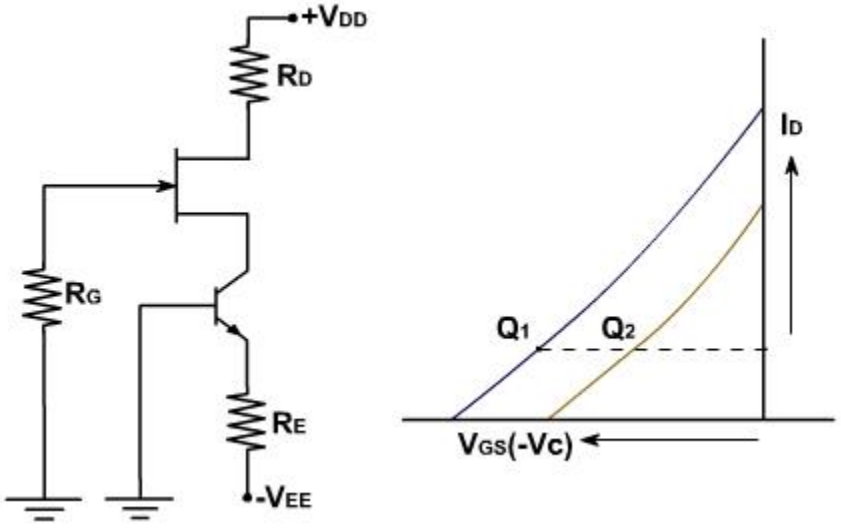


Fig. 4

The bipolar transistor is emitter biased; its collector current is given by

$I_C = (V_{EE} - V_{BE}) / R_E$.

Because the bipolar transistor acts like a current source, it forces the drain current to equal the bipolar collector current.

$I_D = I_C$

Since I_C is constant, both Q points have the same value of drain current. The current source effectively wipes out the influence of V_{GS}. Although V_{GS} is different for each Q point, it no longer influences the value of drain current.

Using One power supply:

When only a positive supply is available, the circuit shown in **fig. 5**, can be used to set up a constant drain current.

In this case, the bipolar transistor is voltage divider biased. Assuming a stiff voltage divider, the emitter and collector currents are constant for all bipolar transistors. This forces the FET drain current equal the bipolar collector current.

$$V_{TH} = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E}$$

Since V_{TH} is constant, I_E is also constant

$$I_C = I_S = I_D = \text{constant}$$

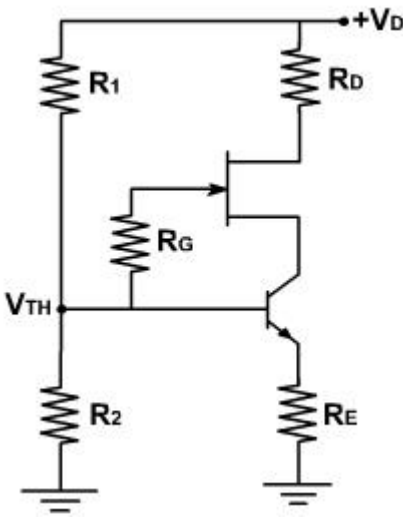


Fig. 5

Transductance:

The transductance of a FET is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{gs}}\right|_{V_{DS}=0} \mu A/Volts$$

Because the changes in I_D and V_{GS} are equivalent to ac current and voltage. This equation can be written as

$$g_m = \left.\frac{i_d}{V_{gs}}\right|_{V_{ds}=0}$$

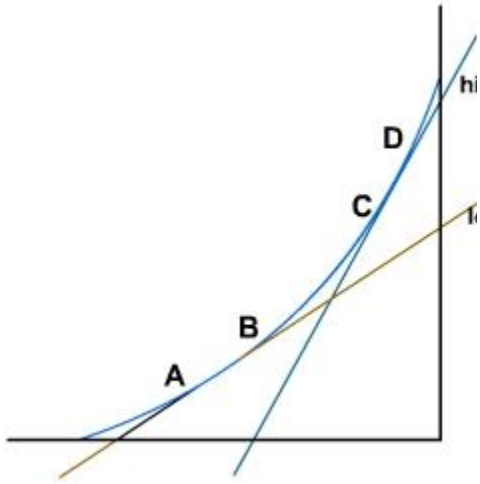


Fig. 6

The unit of g_m is mho or siemems.

Typical value of g_m is 2000 m A / V.

The value of g_m can be obtained from the transductance curve as shown in **fig. 6**.

If A and B points are considered, than a change in V_{GS} produces a change in I_D. The ratio of I_D and V_{GS} is the value of g_m between A and B points. If C and D points are considered, then same change in V_{GS} produces more change in I_D. Therefore, g_m value is higher. In a nutshell, g_m tells us how much control gate voltage has over drain current. Higher the value of g_m, the more effective is gate voltage in controlling gate current. The second parameter r_d is the drain resistance.

$$r_d = \left.\frac{v_{ds}}{i_d}\right|_{V_{gs}=0} \quad (r_d \text{ is negligible})$$

Similar to Bipolar junction transistor. JFET can also be used as an amplifier. The ac equivalent circuit of a JFET is shown in **fig. 1**.

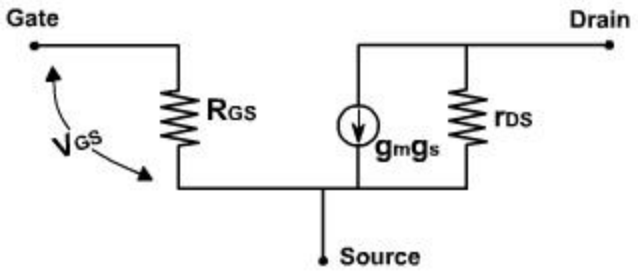


Fig. 1

The resistance between the gate and the source R_{GS} is very high. The drain of a JFET acts like a current source with a value of $g_m V_{gs}$. This model is applicable at low frequencies.

From the ac equivalent model

$$i_d = g_m V_{gs} + \frac{V_{ds}}{r_d}$$

When $i_d = 0$, $\quad \frac{V_{ds}}{V_{gs}} = -g_m r_d$

The amplification factor μ for FET is defined as

$$\mu = \left.\frac{v_{ds}}{v_{gs}}\right|_{i_d=0} \quad \therefore \mu = g_m r_d$$

When $V_{GS} = 0$, g_m has its maximum value. The maximum value is designated as g_{mo}.

Again consider the equation,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]\left[\frac{-1}{V_{GS(off)}}\right]$$

$$g_m = \frac{-2I_{DSS}}{V_{GS(off)}}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

When $\quad V_{GS} = 0,\ g_m = g_{mo} = \frac{-2I_{DSS}}{V_{GS(off)}}$

$$\therefore g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

As V_{GS} increases, gm decreases linearly.

$$V_{GS(off)} = \frac{-2I_{DSS}}{g_{mo}}$$

Measuring I_{DSS} and g_m, $V_{GS(off)}$ can be determined

FET as Amplifier:

Fig. 2, shows a common source amplifier.

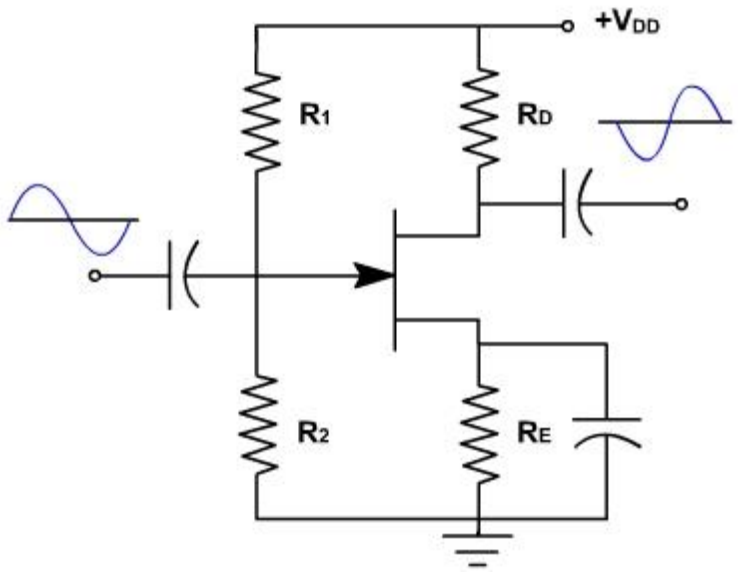


Fig. 2

When a small ac signal is coupled into the gate it produces variations in gate source voltage. This produces a sinusoidal drain current. Since an ac current flows through the drain resistor. An amplified ac voltage is obtained at the output. An increase in gate source voltage produces more drain current, which means that the drain voltage is decreasing. Since the positive half cycle of input voltage produces the negative half cycle of output voltage, we get phase inversion in a CS amplifier.

The ac equivalent circuit is shown in **fig. 3**.

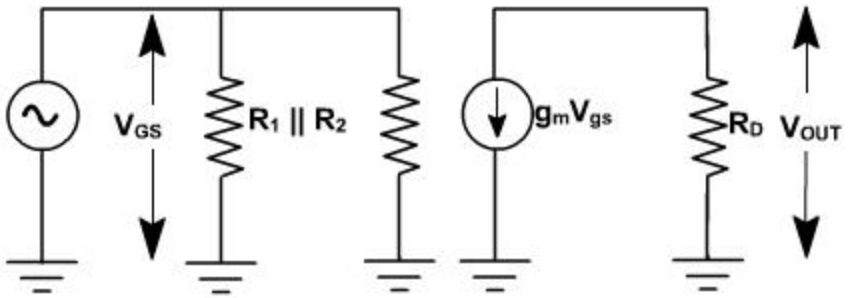


Fig. 3

The ac output voltage is

$v_{out} = - g_m v_{gS} R_D$

Negative sign means phase inversion. Because the ac source is directly connected between the gate source terminals therefore ac input voltage equals

$V_{in} = V_{gs}$

The voltage gain is given by

$$A_V = \frac{v_{out}}{v_{in}} = - g_m R_D$$

$A_V =$ unloaded voltage gain

The further simplified model of the amplifieris shown in **fig. 4**.

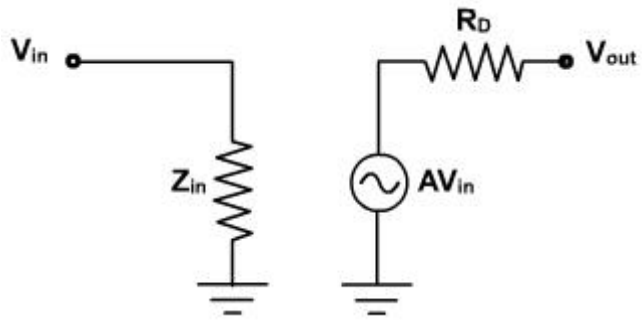


Fig. 4

Z_{in} is the input impedance. At low frequencies, this is parallel combination of R_1|| R_2|| R_{GS}. Since R_{GS} is very large, it is parallel combination of R_1 & R_2. A V_{in} is output voltage and R_D is the output impedance.

Because of nonlinear transductance curve, a JFET distorts large signals, as shown in **fig. 5**.

Given a sinusoidal input voltage, we get a non-sinusoidal output current in which positive half cycle is elongated and negative cycle is compressed. This type of distortion is called Square law distortion because the transductance curve is parabolic.

JFET Applications

Example-1:

Determine gm for an n-channel JFET with characteristic curve shown in **fig. 1**.

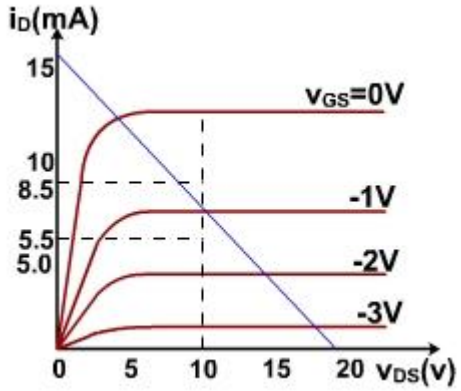


Fig. 1

Solution:

We select an operating region which is approximately in the middle of the curves; that is, between v_{GS} = -0.8 V and v_{GS} = -1.2 V; i_D = 8.5mA and i_D = 5.5 mA. Therefore, the transductance of the JFET is given by

$$g_m = \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_{v_{GS}=\text{constant}} = 7.5\ m\Omega^{-1}$$

Design of JFET amplifier:

To design a JFET amplifier, the Q point for the dc bias current can be determined graphically. The dc bias current at the Q point should lie between 30% and 70% of I_{DSS}. This locates the Q point in the linear region of the characteristic curves.

The relationship between i_D and v_{GS} can be plotted on a dimensionless graph (i.e., a normalized curve) as shown in **fig. 2** .

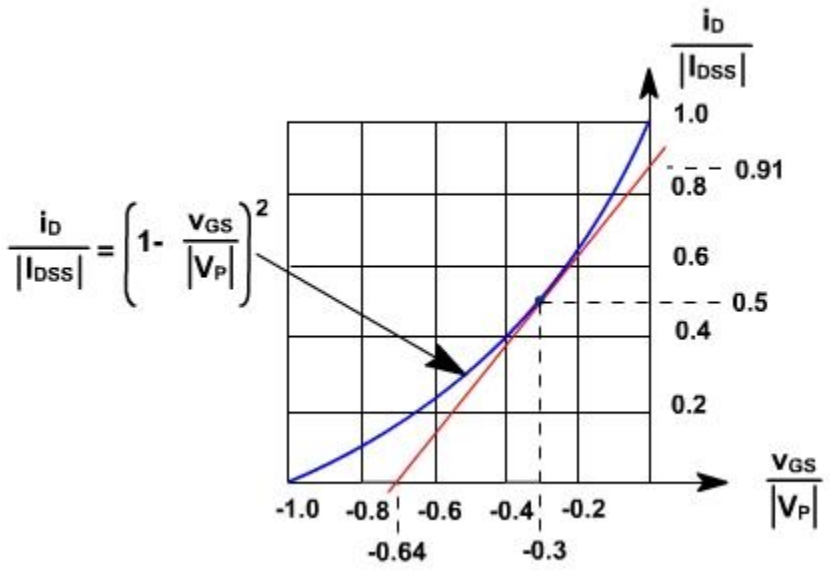


Fig. 2

The vertical axis of this graph is i_D / I_{DSS} and the horizontal axis is v_{GS} / V_P. The slope of the curve is g_m.

A reasonable procedure for locating the quiescent point near the center of the linear operating region is to select $I_{DQ} \approx I_{DSS} / 2$ and $V_{GSQ} \approx 0.3V_P$. Note that this is near the midpoint of the curve. Next we select $v_{DS} \approx V_{DD} / 2$. This gives a wide range of values for v_{ds} that keep the transistor in the pinch ◆off mode.

The transductance at the Q-point can be found from the slope of the curve of **fig.2** and is given by

$$g_m = \frac{1.41\ I_{DSS}}{V_P}$$

Example-2

Determine g m for a JFET where I_{DSS} = 7 mA, V_P = -3.5 V and V_{DD} = 15V. Choose a reasonable location for the Q-point.

Solution:

Let us select the Q-point as given below:

$$I_{DQ} = \frac{I_{DSS}}{2} = 3.5 \text{ mA}$$

$$V_{DSQ} = \frac{V_{DD}}{2} = 7.5 \text{ V}$$

$$V_{GSQ} = 0.3V_P = -1.05 \text{V}$$

The transconductance, g_m, is found from the slope of the curve at the point $i_D / I_{DSS} = 0.5$ and $v_{GS} / V_P = 0.3$. Hence,

$$g_m = \frac{1.41\ I_{DSS}}{V_P} = 2840\ \mu\Omega^{-1}$$

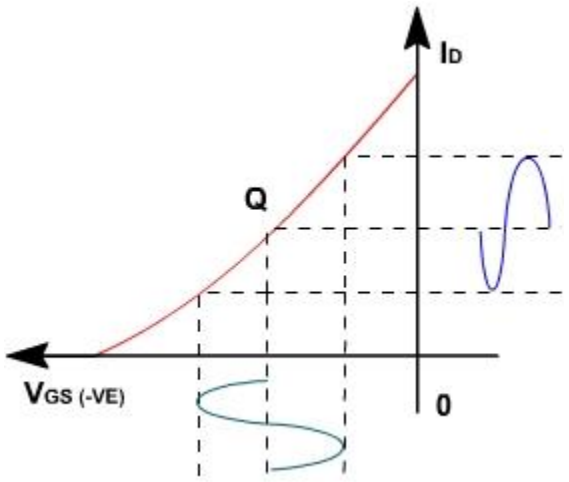


Fig. 5

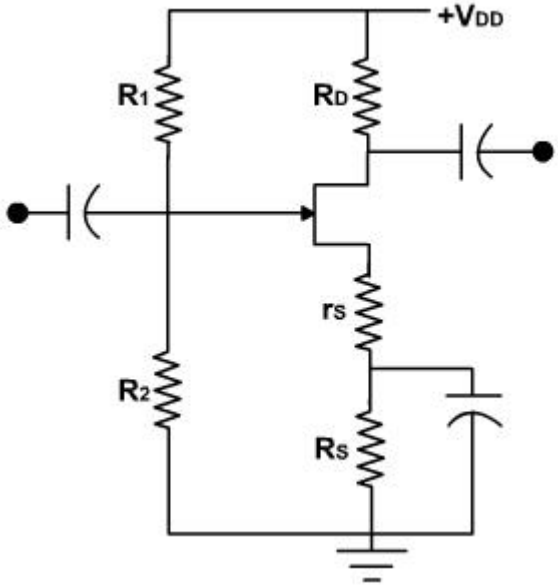


Fig. 6

This distortion is undesirable for an amplifier. One way to minimize this is to keep the signal small. In that case a part of the curve is used and operation is approximately linear. Some times swamping resistor is used to minimize distortion and gain constant. Now the source is no longer ac ground as shown in **fig. 6**.

The drain current through r_S produces an ac voltage between the source and ground. If r_S is large enough the local feedback can swamp out the non-linearity of the curve. Then the voltage gain approaches an ideal value of R_D / r_S.

Since R_{GS} approaches infinity therefore, all the drain current flows through r_S producing a voltage drop of $g_m V_{gS} r_S$. The ac equivalent circuit is shown in **fig. 7**.

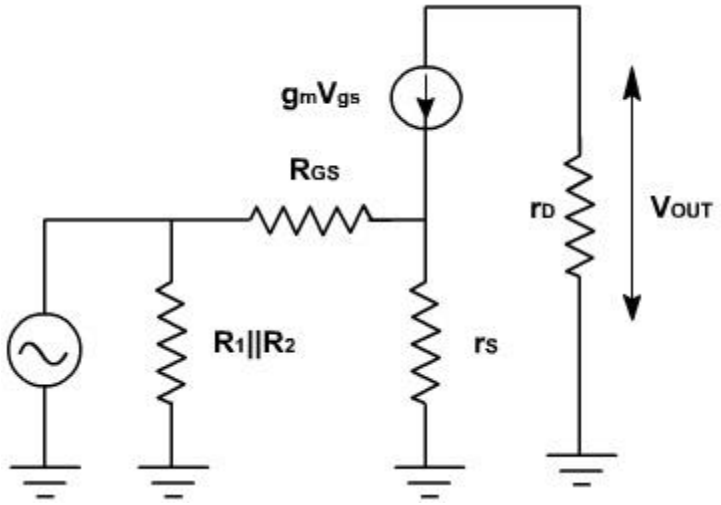


Fig. 7

$$v_{gs} + g_m \, v_{gs} . r_s - v_{in} = 0$$

$$v_{in} = (1 + g_m r_s) \, v_{gs}$$

$$v_{out} = - g_m R_D \, v_{gs}$$

$$A = \frac{- g_m \, R_D}{1 + g_m \, r_s} = \frac{-R_D}{r_s + 1/g_m}$$

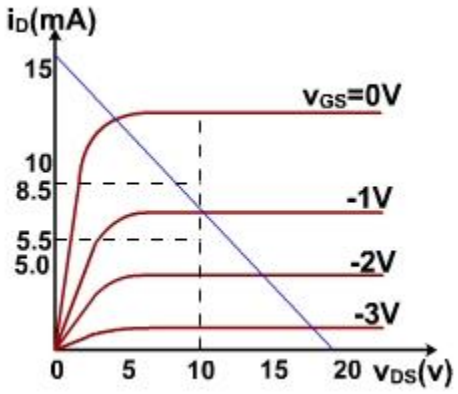
The voltage gain reduces but voltage gain is less effective by change in g_m. r_S must be greater than $1 / g_m$ only then

$$v_{gs} = - \frac{R_D}{r_s}$$

JFET Applications

Example-1:

Determine gm for an n-channel JFET with characteristic curve shown in **fig. 1**.



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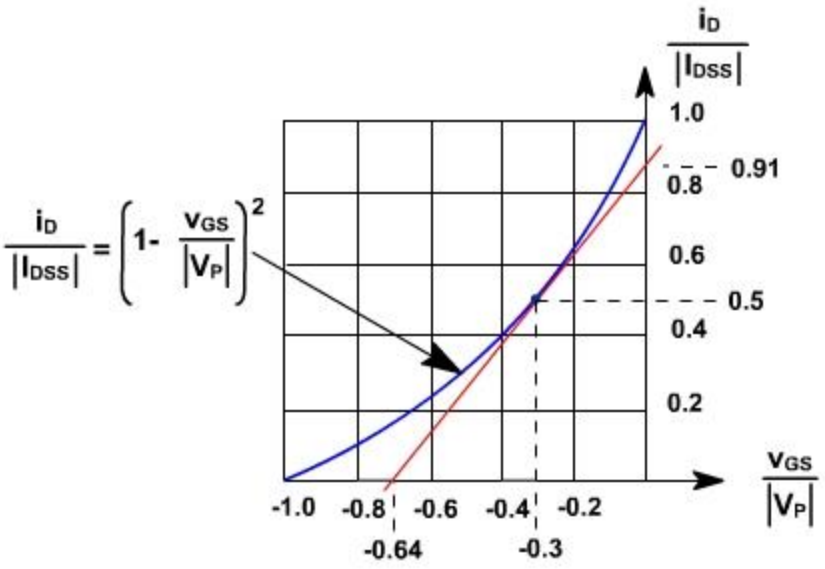

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$$g_m = \frac{1.41\ I_{DSS}}{V_P} = 2840\ \mu\Omega^{-1}$$

JEFT as Analog Switch:

JFET can be used as an analog switch as shown in **fig. 3**. It is the major application of a JFET. The idea is to use two points on the load line: cut off and saturation. When JFET is cut off, it is like an open switch. When it is saturated, it is like a closed switch.

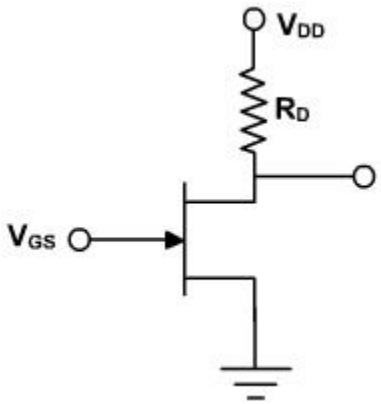

Fig. 3

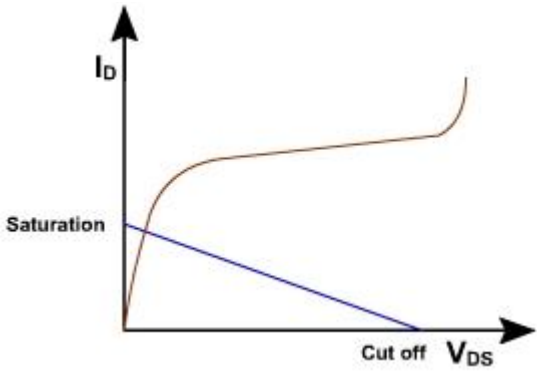

Fig. 4

When $V_{GS} = 0$, the JFET is saturated and operates at the upper end of the load line. When V_{GS} is equal to or more negative than $V_{GS}(off)$, it is cut off and operates at lower end of the load line (open and closed switch).This is shown in **fig. 4**.

Only these two points are used for operation when used as a switch. The JFET is normally saturated well below the knee of the drain curve. For this reason the drain current is much smaller than I_{DSS} .

FET as a Shunt Switch:

FET can be used as a shunt switch as shown in **fig. 5**. When V_{cont}=0, the JFT is saturated and the switch is closed When V_{cont} is more negative FET is like an open switch. The equivalent circuit is also shown in **fig. 5**.

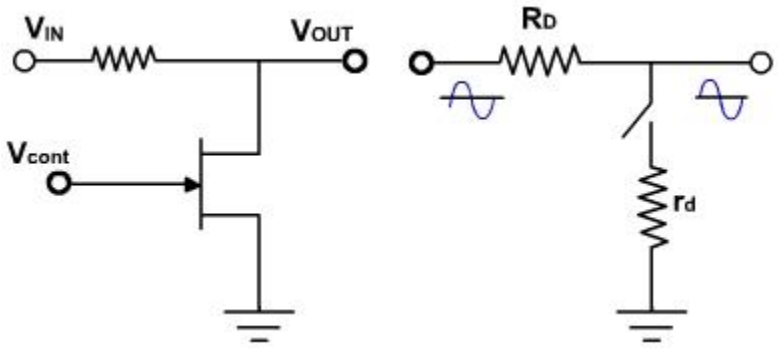

Fig. 5

FET as a series switch:

JFET can also be used as series switch as shown in **fig. 6**. When control is zero, the FET is a closed switch. When V_{con}= negative, the FET is an open switch. It is better than shunt switch.

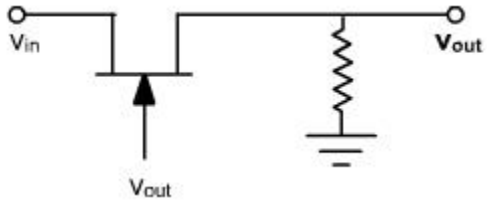

Fig. 6

Multiplexing:

One of the important application of FET is in analog multiplexer. Analog multiplexer is a circuit that selects one of the output lines as shown in **fig. 7**. When control voltages are more negative

all switches are open and output is zero. When any control voltage becomes zero the input is transmitted to the output.

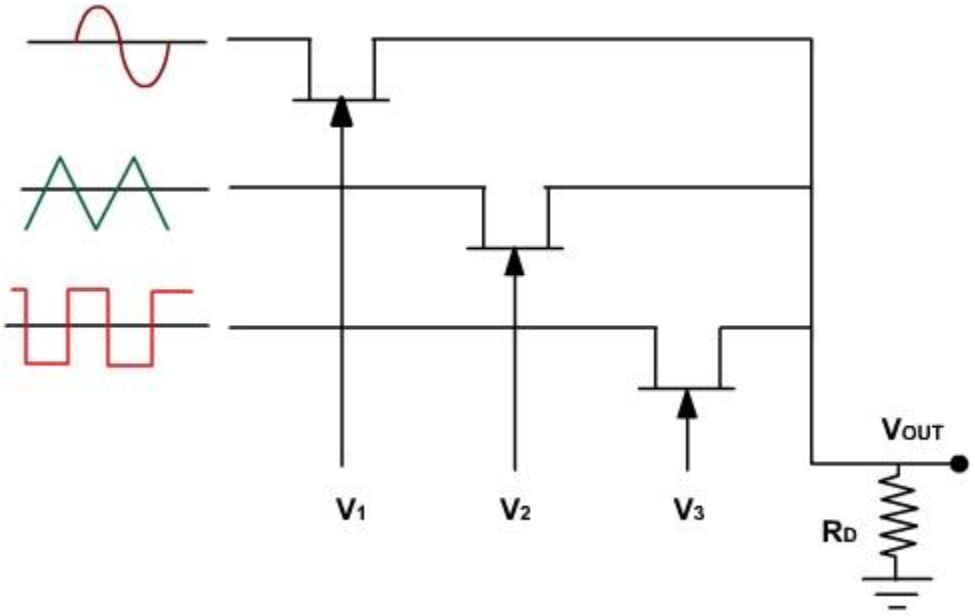

Fig. 7