Chapter 2. - DC Biasing - BJTs

Objectives

To Understand :

•   Concept of Operating point and stability

•   Analyzing Various biasing circuits and their comparison with respect to stability

BJT – A Review

•   Invented in 1948 by Bardeen, Brattain and Shockley

•   Contains three adjoining, alternately doped semiconductor regions: Emitter (E), Base (B), and Collector (C)

•   The middle region, base, is very thin

•   Emitter is heavily doped compared to collector. So, emitter and collector are not interchangeable.

Three operating regions

•   Linear – region operation:

–   Base – emitter junction forward biased

–   Base – collector junction reverse biased

•   Cutoff – region operation:

–   Base – emitter junction reverse biased

–   Base – collector junction reverse biased

•   Saturation – region operation:

– Base – emitter junction forward biased

– Base – collector junction forward biased

Three operating regions of BJT

* Cut off: $VCE = VCC$, $IC \cong 0$

* Active or linear : $VCE \cong VCC/2$, $IC \cong IC\ max/2$

* Saturation: $VCE \cong 0$, $IC \cong IC\ max$

Q-Point (Static Operation Point)
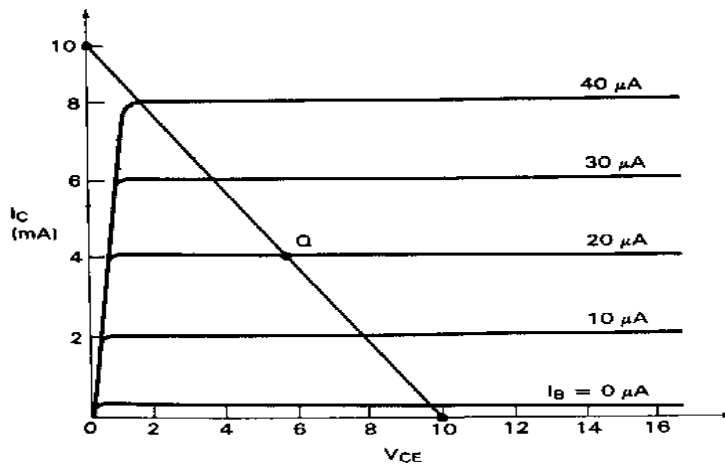
The values of the parameters IB, IC and VCE together are termed as 'operating point' or Q (Quiescent) point of the transistor.

Q-Point

* The intersection of the dc bias value of IB with the dc load line determines the Q- point.

* It is desirable to have the Q-point centered on the load line. Why?

* When a circuit is designed to have a centered Q-point, the amplifier is said to be midpoint biased.

* Midpoint biasing allows optimum ac operation of the amplifier.

Introduction - Biasing

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. In fact, the amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal

- The analysis or design of any electronic amplifier therefore has two components:

- The dc portion and

- The ac portion

During the design stage, the choice of parameters for the required dc levels will affect the ac response.

What is biasing circuit?

- Once the desired dc current and voltage levels have been identified, a network must be constructe1d that will establish the desired values of IB, IC and VCE, Such a network is known as biasing circuit. A biasing network has to preferably make

use of one power supply to bias both the junctions of the transistor.

Purpose of the DC biasing circuit

- To turn the device "ON"

- To place it in operation in the region of its characteristic where the device operates most linearly, i.e. to set up the initial dc values of IB, IC, and VCE
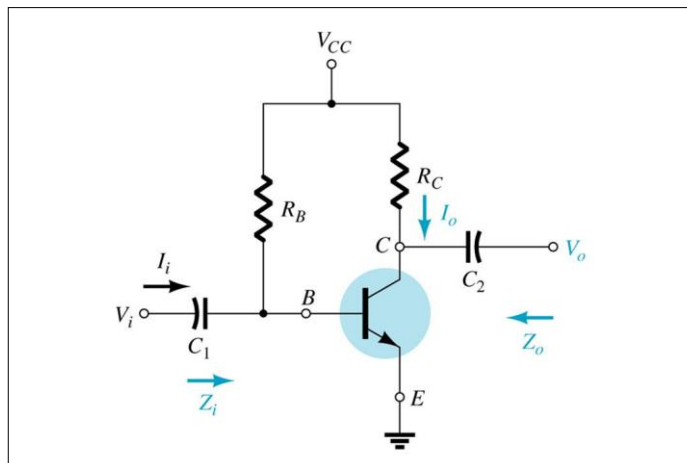
Important basic relationship

- $V_{BE} = 0.7V$

- $I_E = (\beta + 1) I_B \cong I_C$
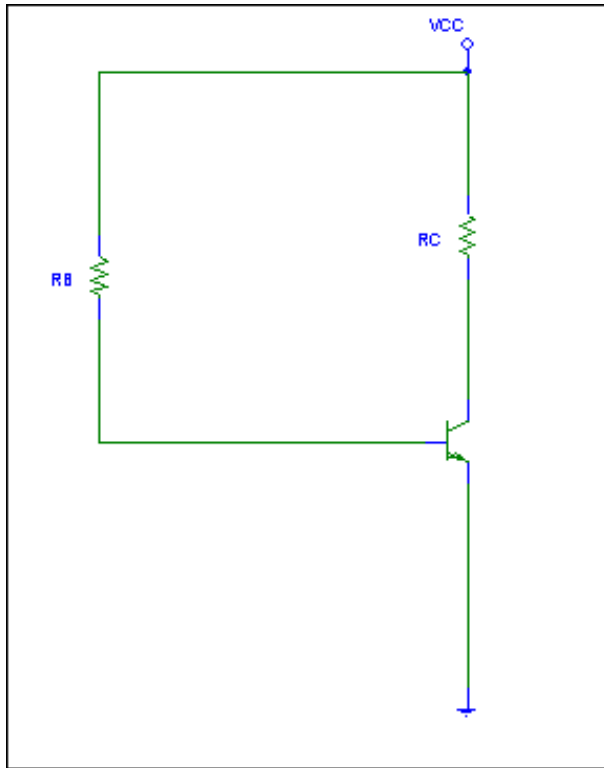
- $I_C = \beta I_B$

Biasing circuits:

- Fixed – bias circuit

- Emitter bias

- Voltage divider bias

- DC bias with voltage feedback

- Miscellaneous bias

Fixed bias

- The simplest transistor dc bias configuration.

- For dc analysis, open all the capacitance.

DC Analysis

•   Applying KVL to the input loop:

$V_{CC} = I_B R_B + V_{BE}$

•   From the above equation, deriving for IB, we get,

$I_B = [V_{CC} - V_{BE}] / R_B$

•   The selection of RB sets the level of base current for the operating point.

•   Applying KVL for the output loop:

$V_{CC} = I_C R_C + V_{CE}$

Thus, $V_{CE} = V_{CC} - I_C R_C$

•   In circuits where emitter is grounded,

$V_{CE} = V_E$

$V_{BE} = V_B$

Design and Analysis

•   Design: Given – IB, IC , VCE and VCC, or IC , VCE and β, design the values of RB, RC using the equations obtained by applying KVL to input and output loops.

•   Analysis: Given the circuit values (VCC, RB and RC), determine the values of IB,

IC , VCE using the equations obtained by applying KVL to input and output loops.

Problem – Analysis

Given the fixed bias circuit with VCC = 12V, RB = 240 kΩ, RC = 2.2 kΩ and β = 75. Determine the values of operating point.

Equation for the input loop is:

IB   = [VCC – VBE] / RB where VBE = 0.7V, thus substituting the other given values in the equation, we get

IB   = 47.08uA

IC = βIB = 3.53mA

VCE = VCC – ICRC = 4.23V

•   When the transistor is biased such that IB is very high so as to make IC very high

such that ICRC drop is almost VCC and VCE is almost 0, the transistor is said to be

in saturation.

IC sat = VCC / RC   in a fixed bias circuit.

Verification

•   Whenever a fixed bias circuit is analyzed, the value of ICQ obtained could be verified with the value of ICSat (= VCC / RC) to understand whether the transistor is in active region.

•   In active region,

ICQ = (ICSat /2)

Load line analysis

A fixed bias circuit with given values of VCC, RC and RB can be analyzed (means, determining the values of IBQ, ICQ and VCEQ) using the concept of load line also.

Here the input loop KVL equation is not used for the purpose of analysis, instead, the output characteristics of the transistor used in the given circuit and output loop KVL equation are made use of.

• The method of load line analysis is as below:

1. Consider the equation VCE = VCC – ICRC This relates VCE and IC for the given IB

and RC

2. Also, we know that, VCE and IC are related through output characteristics

We know that the equation,

VCE = VCC – ICRC

represents a straight line which can be plotted on the output characteristics of the

transistor.

Such line drawn as per the above equation is known as load line, the slope of which is decided by the value of RC (the load).

Load line

(a)
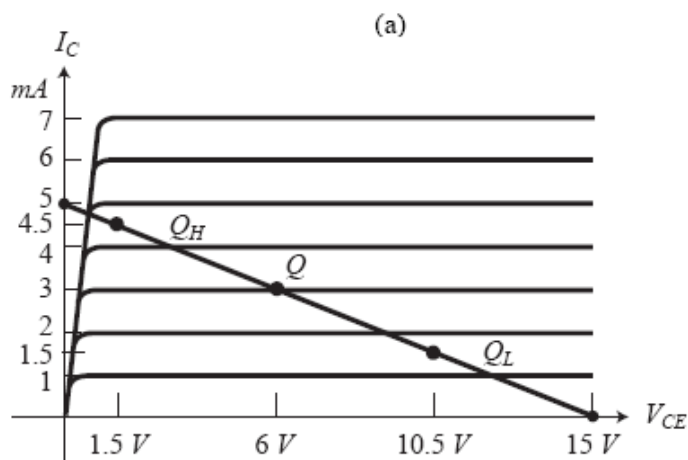
- The two extreme points on the load line can be calculated and by joining which the load line can be drawn.

- To find extreme points, first, Ic is made 0 in the equation: $V_{CE} = V_{CC} - I_C R_C$.

This gives the coordinates $(V_{CC}, 0)$ on the x axis of the output characteristics.

- The other extreme point is on the y-axis and can be calculated by making $V_{CE} = 0$

in the equation $V_{CE} = V_{CC} - I_C R_C$ which gives $I_C(max) = V_{CC} / R_C$ thus giving the

coordinates of the point as $(0, V_{CC} / R_C)$.

- The two extreme points so obtained are joined to form the load line.

- The load line intersects the output characteristics at various points corresponding to different I_Bs. The actual operating point is established for the given I_B.

Q point variation

As I_B is varied, the Q point shifts accordingly on the load line either up or down depending on I_B increased or decreased respectively.

As R_C is varied, the Q point shifts to left or right along the same I_B line since the slope of the line varies. As R_C increases, slope reduces (slope is $-1/R_C$) which results in shift of Q point to the left meaning no variation in I_C and reduction in V_{CE}.

Thus if the output characteristics is known, the analysis of the given fixed bias circuit

or designing a fixed bias circuit is possible using load line analysis as mentioned above.

Emitter Bias

- It can be shown that, including an emitter resistor in the fixed bias circuit improves the stability of Q point.

- Thus emitter bias is a biasing circuit very similar to fixed bias circuit with an emitter resistor added to it.
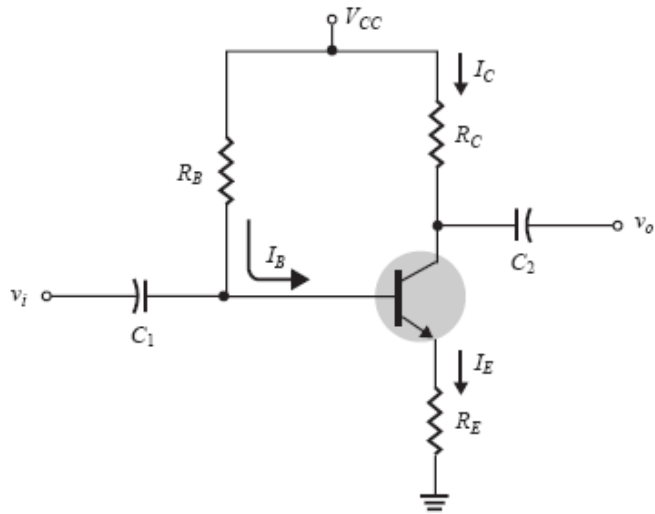
Input loop
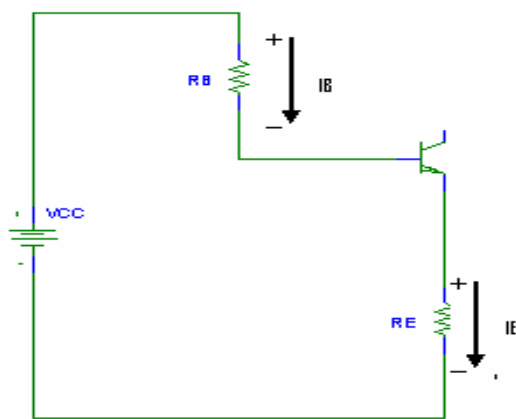
- Writing KVL around the input loop we get,

$$VCC = IBRB + VBE + IERE \quad (1)$$

We know that,

$$IE = (\beta+1)IB \quad (2)$$

Substituting this in (1), we get,

VCC = IBRB + VBE + (β+1)IBRE

VCC – VBE = IB(RB + (β+1) RE)

Solving for IB:

IB = (VCC – VBE) /[(RB + (β+1) RE)]

The expression for IB in a fixed bias circuit was,

IB = (VCC – VBE) /RB

Equivalent   input loop:
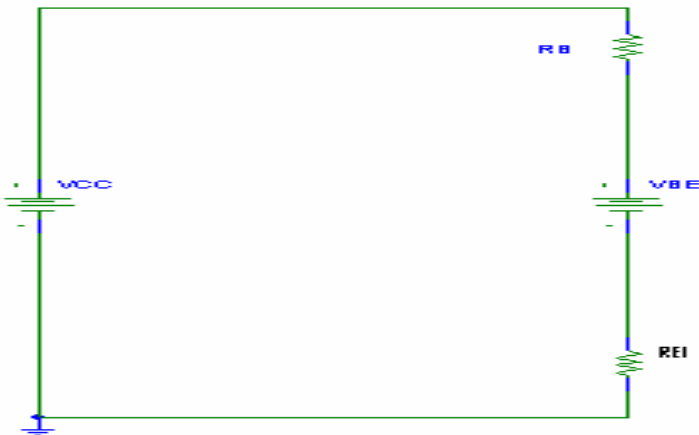
•   REI   in the above circuit is (β+1)RE which means that, the emitter resistance that is common to both the loops appears as such a high resistance in the input loop.

•   Thus Ri = (β+1)RE (more about this when we take up ac analysis)

Output loop
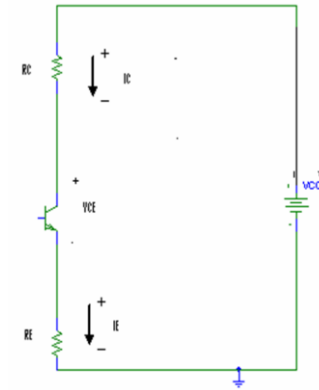
Collector – emitter loop

Applying KVL,

VCC = ICRC + VCE + IERE

I_C is almost same as I_E

Thus,

VCC = ICRC + VCE + ICRE

= IC (RC + RE) +VCE

VCE = VCC - IC (RC + RE)

Since emitter is not connected directly to ground, it is at a potential VE, given by,

VE = IERE

VC = VCE + VE OR VC = VCC – ICRC

Also, VB = VCC – IBRB OR VB = VBE + VE

Problem:

Analyze the following circuit: given

$\beta = 75$, VCC = 16V, RB = 430kΩ, RC = 2kΩ and RE = 1k Ω
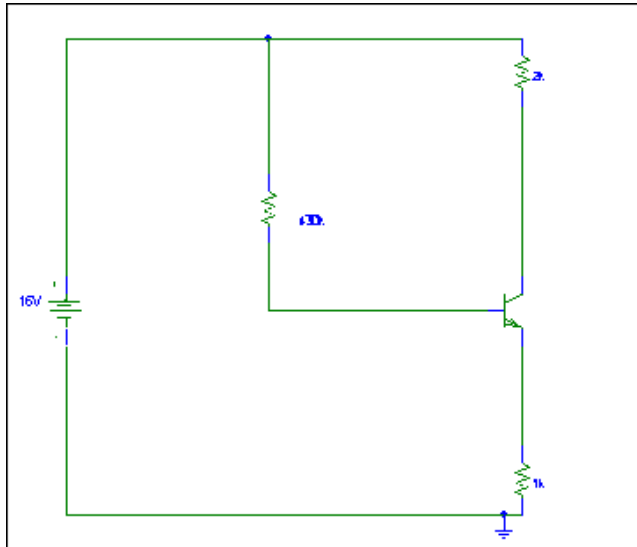
Solution:

IB = (VCC − VBE) /[(RB + (β+1) RE)]

= (16 − 0.7) / [430k + (76) 1k] = 30.24μA

IC = (75) (30.24μA) = 2.27mA

VCE = VCC - IC (RC + RE) = 9.19V VC = VCC − ICRC = 11.46V

VE = VC − VCE = 2.27V VB = VBE + VE = 2.97V

VBC = VB − VC = 2.97 − 11.46 = - 8.49V

Improved bias stability

•   Addition of emitter resistance makes the dc bias currents and voltages remain closer to their set value even with variation in

–   transistor beta

–   temperature

Stability

In a fixed bias circuit, IB does not vary with β and therefore whenever there is an increase in β, IC increases proportionately, and thus VCE reduces making the Q point to drift towards saturation. In an emitter bias circuit, As β increases, IB reduces, maintaining almost same IC and VCE thus stabilizing the Q point against β variations.

Saturation current
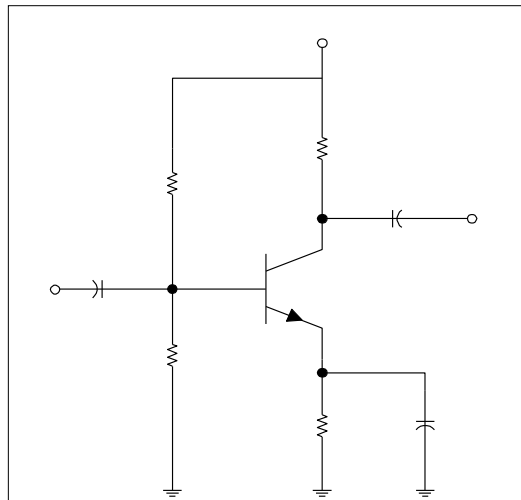
In saturation VCE is almost 0V,

Thus, saturation current

VCC = IC (RC + RE)

ICsat = VCC / (RC + RE)

Load line analysis

The two extreme points on the load line of an emitter bias circuit are, (0, VCC / [RC + RE]) on the Y axis, and (VCC, 0) on the X axis.

Voltage divider bias

This is the biasing circuit wherein, ICQ and VCEQ are almost independent of β. The level of IBQ will change with β so as to maintain the values of ICQ and VCEQ almost same, thus maintaining the stability of Q point.

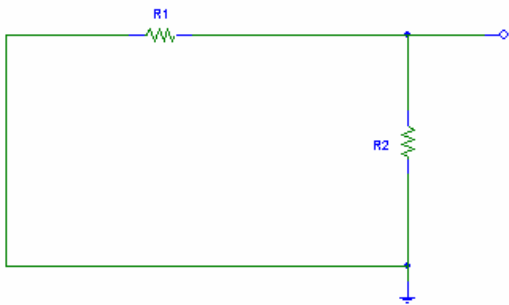Two methods of analyzing a voltage divider bias circuit are:

Exact method – can be applied to any voltage divider circuit Approximate method – direct method, saves time and energy, can be applied in most of the circuits.

Exact method

In this method, the Thevenin equivalent network for the network to the left of the base terminal to be found.
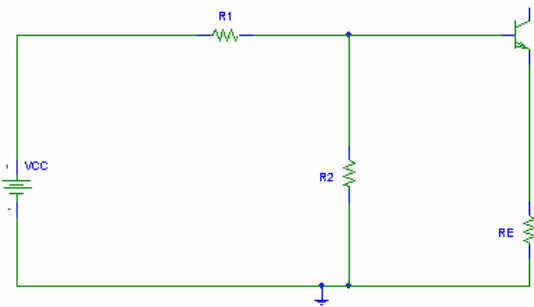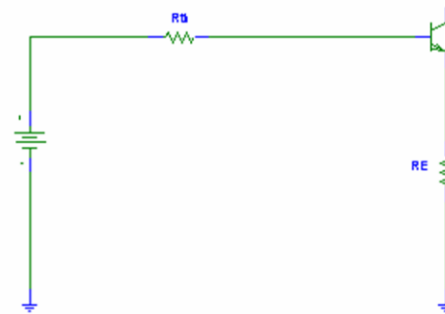

To find Rth:

From the above circuit,

Rth = R1|| R2

= R1 R2 / (R1 + R2)

To find Eth
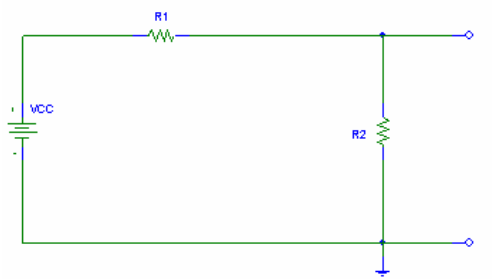
From the above circuit,

Eth = VR2 = R2VCC / (R1 + R2)

In the above network, applying KVL

(Eth − VBE) = IB [Rth +(β + 1) RE] IB   = (Eth − VBE) / [Rth +(β + 1) RE]

Analysis of Output loop
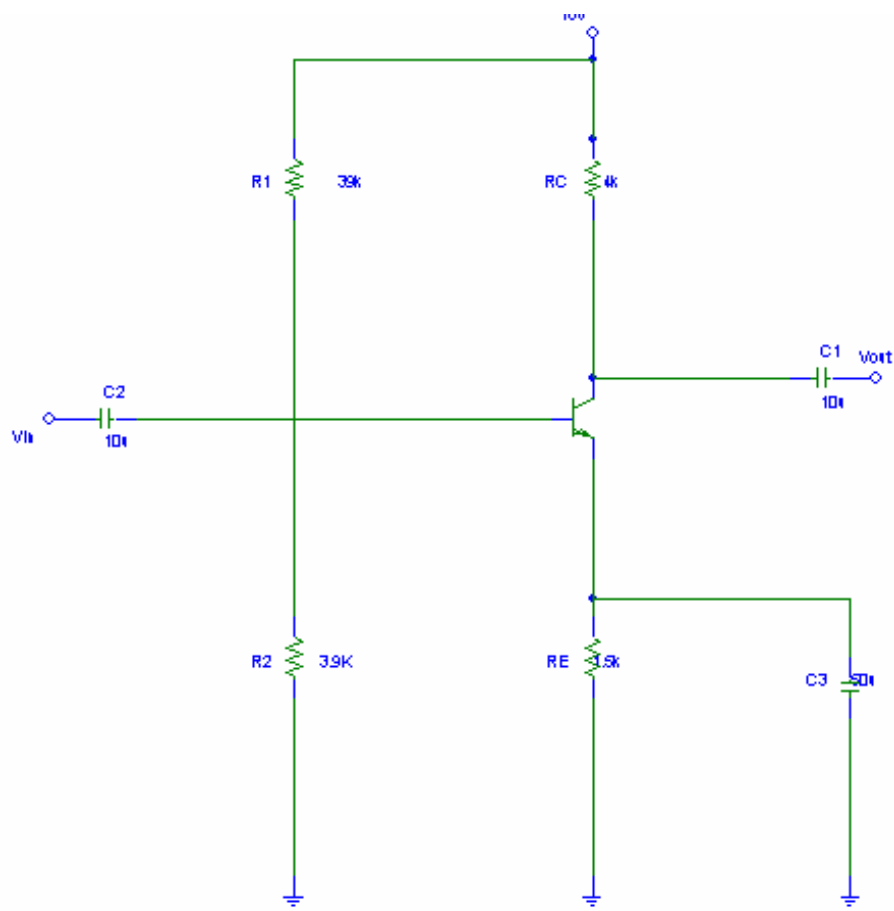
KVL to the output loop:

$$VCC = ICRC + VCE + IERE$$

$$IE \cong IC$$

Thus, $VCE = VCC - IC (RC + RE)$ Note that this is similar to emitter bias circuit.

Problem

For the circuit given below, find IC and VCE.

Given the values of R1, R2, RC, RE and $\beta = 140$ and VCC = 18V.

For the purpose of DC analysis, all the capacitors in the amplifier circuit are opened.

Solution:

Considering exact analysis:

1. Let us find   Rth = R1|| R2

= R1 R2 / (R1 + R2) = 3.55K

2. Then find   Eth = VR2 = R2VCC / (R1 + R2)

3. Then find IB

= 1.64V

IB   = (Eth − VBE) / [Rth +(β + 1) RE]
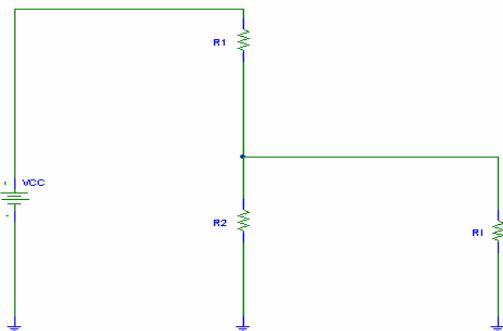
= 4.37µA

4. Then find   IC = β IB = 0.612mA

5. Then find   VCE = VCC − IC (RC + RE)

= 12.63V

Approximate analysis:

The input section of the voltage divider configuration can be represented by the network shown below.

Input Network

The emitter resistance RE is seen as (β+1)RE at the input loop.

If this resistance is much higher compared to R2, then the current IB is much smaller than

I2 through R2.

This means,   Ri >> R2

OR

$(\beta+1)RE \geq 10R2$

OR

$\beta RE \geq 10R2$

This makes IB to be negligible. Thus I1 through R1 is almost same as the current I2 through R2.

Thus R1 and R2 can be considered as in series. Voltage divider can be applied to find the voltage across R2 (VB)

$VB = VCCR2 / (R1 + R2)$ Once VB is determined, VE is calculated as,

$VE = VB - VBE$

After finding VE, IE is calculated as,

$IE = VE / RE$

$IE \cong IC$

$VCE = VCC - IC (RC + RE)$

Problem

Given: VCC = 18V, R1 = 39k Ω, R2 = 3.9k Ω, RC = 4k Ω, RE = 1.5k Ω and β = 140. Analyse the circuit using approximate technique.

In order to check whether approximate technique can be used, we need to verify the condition,

$\beta RE \geq 10R2$

Here,

βRE = 210 kΩ and 10R2 = 39 kΩ

Thus the condition $\beta R_E \geq 10 R_2$ satisfied

Solution

-      Thus approximate technique can be applied.

1. Find $V_B = V_{CC} R_2 / (R_1 + R_2) = 1.64V$

2. Find $V_E = V_B - 0.7 = 0.94V$

3. Find $I_E = V_E / R_E = 0.63mA = I_C$

4. Find $V_{CE} = V_{CC} - I_C(R_C + R_E) = 12.55V$

Comparison

Both the methods result in the same values for IC and VCE since the condition $\beta R_E \geq$
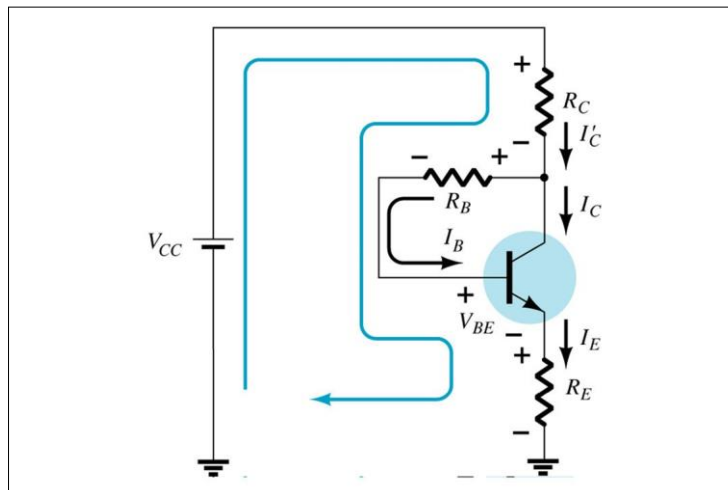
10R2 is satisfied.

It can be shown that the results due to exact analysis and approximate analysis have

more deviation if the above mentioned condition is not satisfied.

For load line analysis of voltage divider network, Ic,max = VCC/ (RC+RE) when VCE

= 0V and VCE max = VCC when IC = 0.

DC bias with voltage feedback
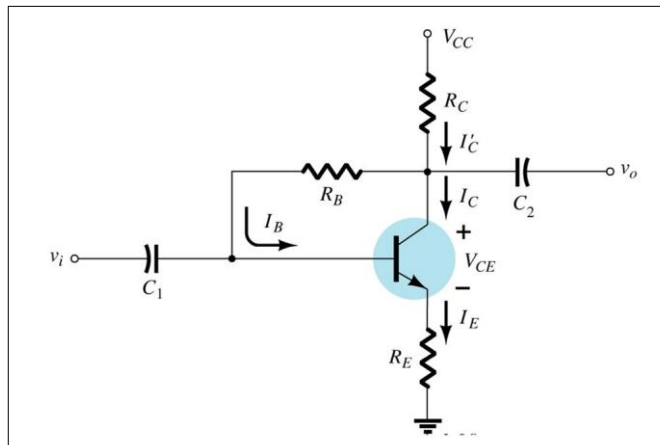
Input loop
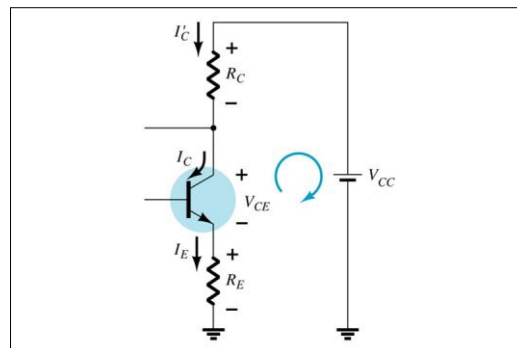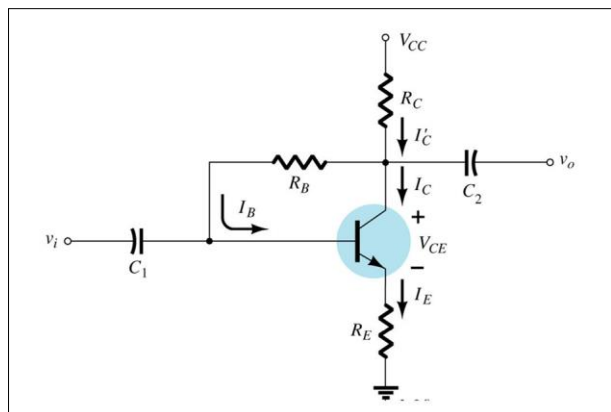

Applying KVL for Input Loop:

VCC = IC1RC + IBRB + VBE + IERE

Substituting for IE as $(\beta +1)$IB and solving for IB, IB = (VCC − VBE) / [RB + β(RC + RE)]
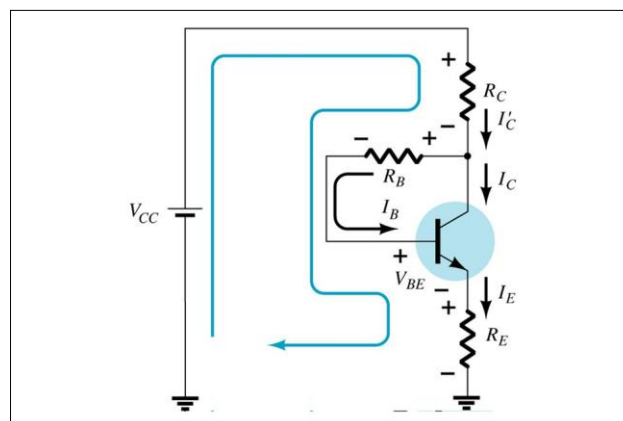
Output loop

Neglecting the base current, KVL to the output loop results in, VCE = VCC – IC (RC + RE)

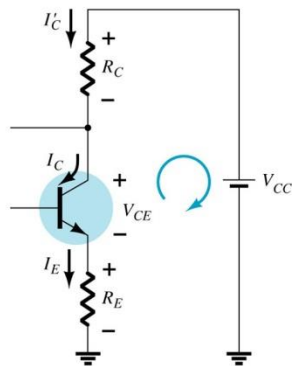DC bias with voltage feedback

Input loop

Applying KVL to input loop:

VCC = IC|RC + IBRB + VBE + IERE

IC| $\cong$ IC and IC $\cong$ IE

Substituting for IE as (β +1)IB [or as βIB] and solving for IB,

IB = (VCC – VBE) / [RB + β(RC + RE)]

Output loop

Neglecting the base current, and applying KVL to the output loop results in,

VCE = VCC – IC (RC + RE)

In this circuit, improved stability is obtained by introducing a feedback path from collector to base.

Sensitivity of Q point to changes in beta or temperature variations is normally less than that encountered for the fixed bias or emitter biased configurations.

Problem:

Given:

VCC = 10V, RC = 4.7k, RB = 250Ω and RE = 1.2k. β = 90. Analyze the circuit.

IB = (VCC – VBE) / [RB + β(RC + RE)]

$= 11.91\mu A$

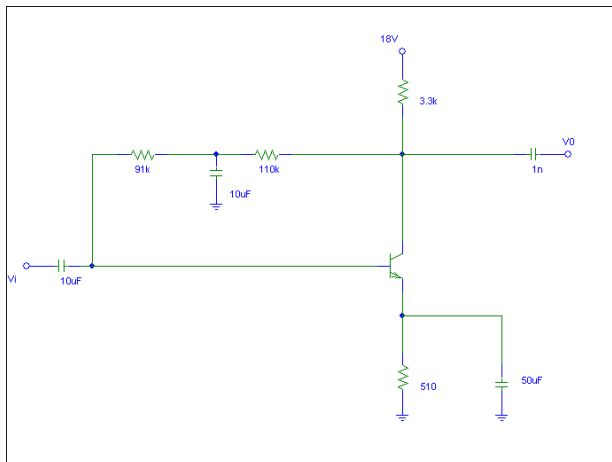$IC = (\beta\ IB\ ) = 1.07mA$

$VCE = VCC - IC\ (\ RC + RE) = 3.69V$

In the above circuit, Analyze the circuit if $\beta = 135$ (50% increase). With the same procedure as followed in the previous problem, we get

- IB = 8.89μA

- IC = 1.2mA

- VCE = 2.92V

50% increase in β resulted in 12.1% increase in IC and 20.9% decrease in VCEQ

Problem 2:

Determine the DC level of IB and VC for the network shown:

Solution:

Open all the capacitors for DC analysis.

RB = 91 kΩ + 110 kΩ = 201k

IB = (VCC – VBE) / [RB + β(RC + RE)]

= (18 – 0.7) / [201k + 75(3.3+0.51)]

= 35.5µA

IC = β IB   = 2.66mA

VCE = VCC – (ICRC)

= 18 – (2.66mA)(3.3k)

= 9.22V

Load line analysis

The two extreme points of the load line $I_{C,max}$ and V_{CE}, max are found in the same as a voltage divider circuit.
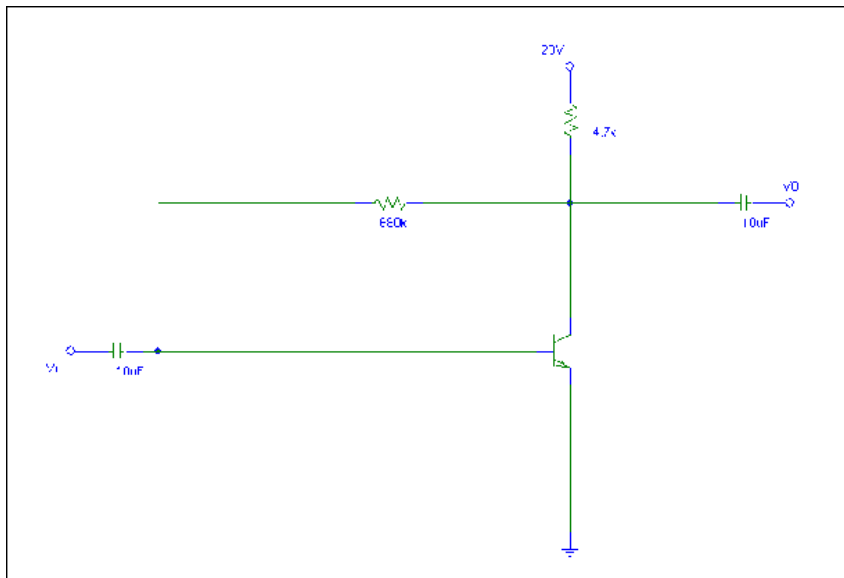
$I_{C,max}$ = VCC / (RC + RE) – Saturation current

V_{CE}, max – Cut off voltage

Miscellaneous bias configurations

There are a number of BJT bias configurations that do not match the basic types of biasing that are discussed till now.

Miscellaneous bias (1)

Analyze the circuit in the next slide. Given $\beta = 120$

Solution

This circuit is same as DC bias with voltage feedback but with no emitter resistor. Thus the expression for IB is same except for RE term.

$IB = (VCC – VBE) / (RB + \beta RC)$
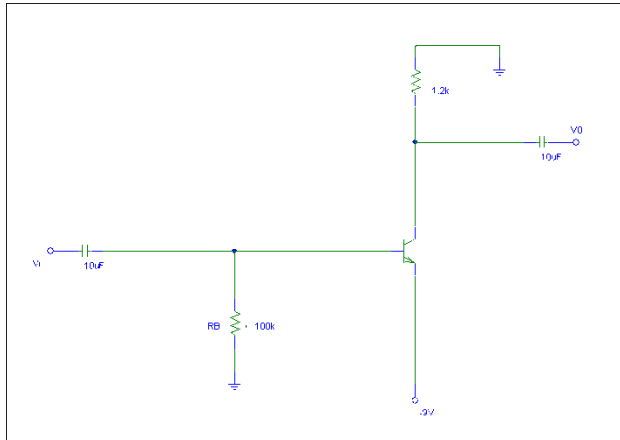
$= (20 – 0.7) / [680k + (120)(4.7k)]$

$= 15.51\mu A$

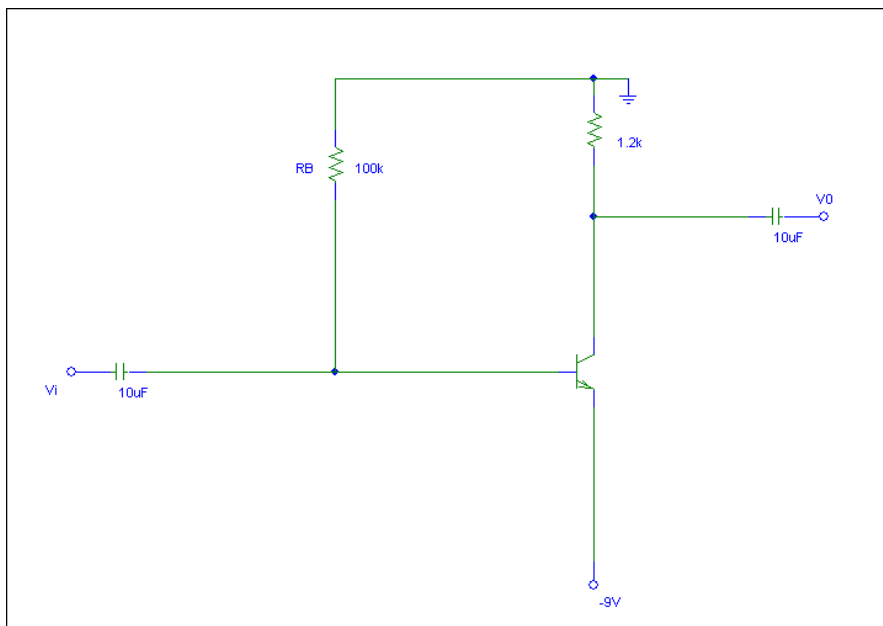$IC = \beta IB = 1.86mA$

$VCE = VCC – ICRC = 11.26V = VCE$

$VB = VBE = 0.7V$
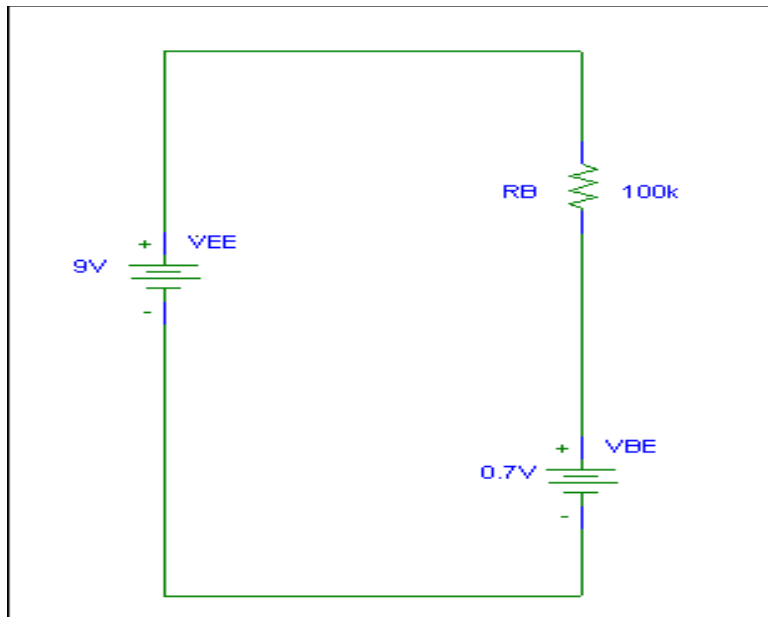
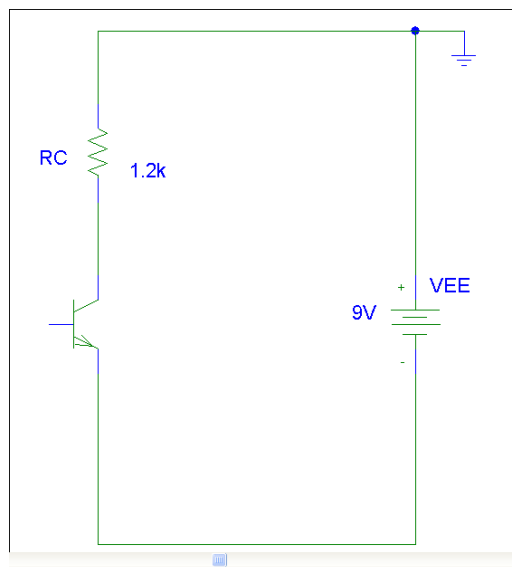$VBC = VB - VC = 0.7V - 11.26V = -10.56V$

Miscellaneous bias (2)

Equivalent circuit

Input loop

Output Loop

Solution

The above circuit is fixed bias circuit. Applying KVL to input loop:

VEE = VBE + IBRB

IB = (VEE – VBE) / RB = 83μA   IC = βIB = 3.735mA

VC = -ICRC = - 4.48V   VB = - IBRB = - 8.3V

Design Operations:

Designing a circuit requires

- Understanding of the characteristics of the device
- The basic equations for the network
- Understanding of Ohms law, KCL, KVL
- If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design.

- Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen.

- Operating point needs to be recalculated with the standard values of resistors chosen and generally the deviation expected would be less than or equal to

5%.

Problem:

- Given $I_{CQ} = 2mA$ and $V_{CEQ} = 10V$. Determine R1 and RC for the network shown:
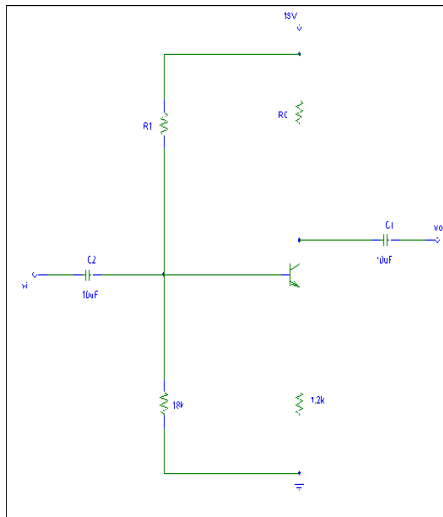
Solution

To find R1:

1.   Find VB. And to find VB, find VE because, VB = VE + VBE

2.   Thus, VE = IERE and IE $\cong$ IC = 2mA

= (2mA)(1.2k) = 2.4V

3. VB =2.4 + 0.7 = 3.1V

4.   Also, VB = VCCR2 /(R1 + R2)

3.1 = (18)(18k) / R1+18k

Thus, R1 = 86.52kΩ

To find RC :

Voltage across RC = VCC – (VCE + IERE)

= 18 – [10 + (2mA)1.2k]

= 5.6V

RC = 5.6/2mA

= 2.8KΩ

Nearest standard values are,

R1 = 82kΩ + 4.7 kΩ = 86.7 k Ω where as calculated value is 86.52 k Ω .

RC = 2.7k in series with 1k = 2.8k both would result in a very close value to the design level.

Problem 2

The emitter bias circuit has the following specifications: ICQ = 1/2Isat, Isat = 8mA, VC =

18V, VCC = 18V and β = 110. Determine RC , RE and RB.

Solution:

        ICQ = 4mA

VRC = (VCC – VC) = 10V RC = VRC / ICQ,

= 10/4mA = 2.5kΩ

To find RE: I_{Csat} = VCC / (RC + RE)

To find RB: Find IB where, IB = IC / β = 36.36µA Also, for an emitter bias circuit,

IB = (VCC – VBE) / RB+(β +1) RE

Thus, RB = 639.8 kΩ

Standard values: RC = 2.4 kΩ, RE = 1 kΩ, RB = 620 kΩ

8mA = 28 / (2.5k + RE) Thus, RE = 1kΩ

Transistor switching networks:

Through proper design transistors can be used as switches for computer and control applications.

When the input voltage VB is high (logic 1), the transistor is in saturation (ON). And the output at its collector = VCE is almost 0V(Logic 0)

Transistor as a switch

When the base voltage VB is low(logic 0), i.e, 0V, the transistor is cutoff(Off) and I_C is 0, drop across RC is 0 and therefore voltage at the collector is VCC. (logic 1)

Thus transistor switch operates as an inverter. This circuit does not require any DC bias at the base of the transistor.

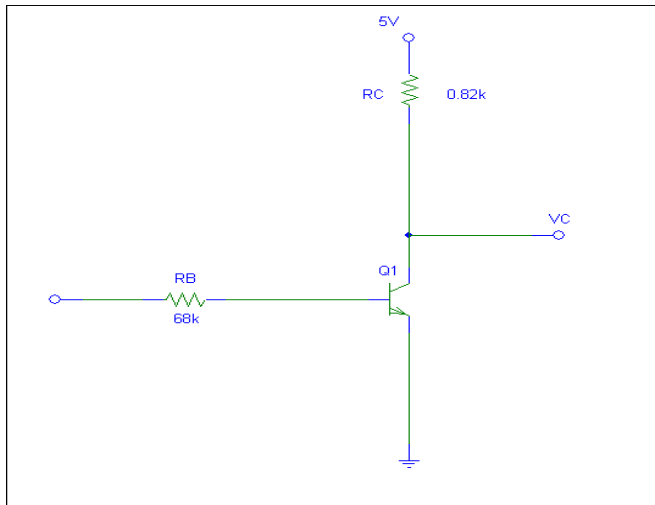Design

When V_i (VB) is 5V, transistor is in saturation and I_{Csat}

Just before saturation, $I_{B,max} = I_{C,sat} / \beta_{DC}$

Thus the base current must be greater than IB,max to make the transistor to work in saturation.

Analysis

When Vi = 5V, the resulting level of IB is

Verification

IB = (Vi – 0.7) / RB

= (5 – 0.7) / 68k

= 63μA

ICsat = VCC / RC = 5/0.82k

= 6.1mA

($I_{C,sat}$ / β) = 48.8μA

Thus IB > (IC,sat / β) which is required for a transistor to be in saturation.

A transistor can be replaced by a low resistance Rsat when in saturation (switch on) Rsat = VCE sat/ ICsat (VCE sat is very small and ICsat is IC,max is maximum current)

A transistor can be replaced by a high resistance Rcutoff when in cutoff (switch on)

Problem

Determine RB and RC for the inverter of figure:
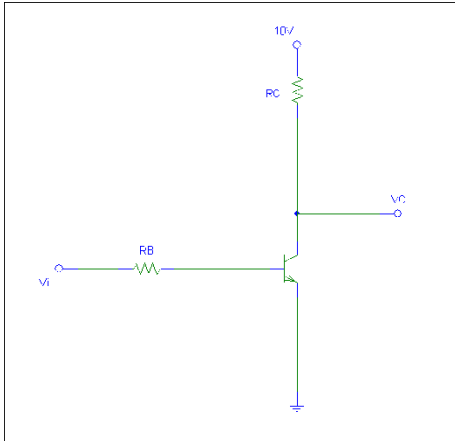
IC sat = VCC / RC

10mA = 10V/ RC

RC = 1kΩ

IB just at saturation = IC sat / β

= 10mA / 250

= 40μA

Choose IB> IC sat / β, 60 μA

IB = (Vi − 0.7) / RB

60 μA = (10 − 0.7) / RB

RB = 155kΩ

Choose RB = 150kΩ, standard value,

re calculate IB, we get IB = 62 μA which is also >   IC sat / β

Thus, RC = 1k and RB = 155k

Switching Transistors

Transistor 'ON' time = delay time + Rise time

Delay time is the time between the changing state of the input and the beginning of a response at the output.

Rise time is the time from 10% to 90% of the final value. Transistor 'OFF' time = Storage time + Fall time

For an 'ON' transistor, VBE should be around 0.7V

For the transistor to be in active region, VCE is usually about 25% to 75% of VCC.

If VCE = almost VCC, probable faults:

–   the device is damaged

–   connection in the collector – emitter or base – emitter circuit loop is open. One of the most common mistake in the lab is usage of wrong resistor value.

Check various voltages with respect to ground.

Calculate the current values using voltage readings rather than measuring current by breaking the circuit.

Problem – 1

Check the fault in the circuit given.
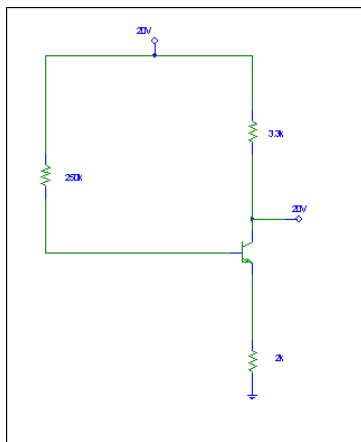
Problem - 2
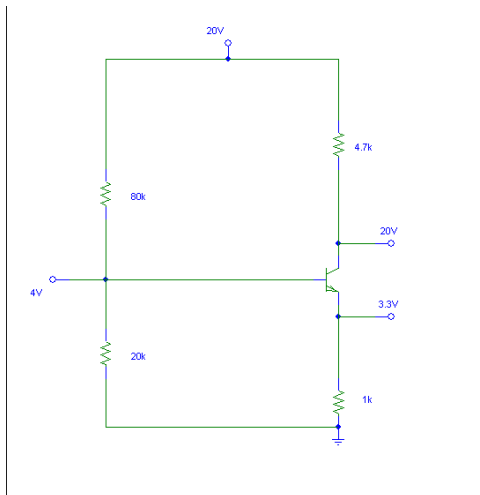
PNP transistors

The analysis of PNP transistors follows the same pattern established for NPN transistors. The only difference between the resulting equations for a network in which an npn transistor has been replaced by a pnp transistor is the sign associated with particular quantities.

PNP transistor in an emitter bias

Applying KVL to Input loop: VCC = IBRB +VBE+IERE

Thus, IB = (VCC – VBE) / [RB + (β+1) RE]

Applying KVL Output loop: VCE = - (VCC – ICRC)

Bias stabilization

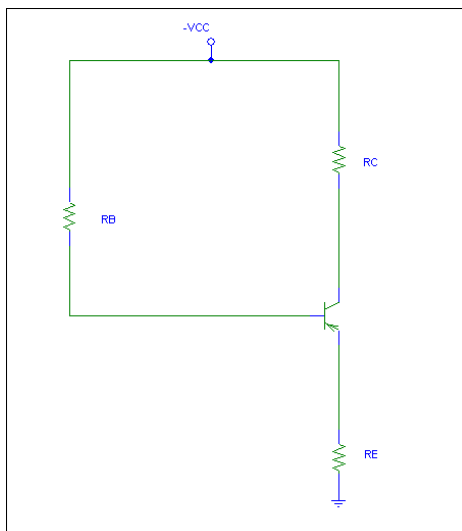The stability of a system is a measure of the sensitivity of a network to variations in its parameters.

In any amplifier employing a transistor the collector current IC is sensitive to each of the following parameters.

β increases with increase in temperature.

Magnitude of VBE decreases about 2.5mV per degree Celsius increase in

temperature.

ICO doubles in value for every 10 degree Celsius increase in temperature.

T (degree Celsius)	Ico (nA)	β	VBE (V)
- 65	0.2 x 10-3	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3 x 103	120	0.3

Stability factors

$S(ICO) = \Delta IC / \Delta IC0$

$S(VBE) = \Delta IC / \Delta VBE$

$S(\beta) = \Delta IC / \Delta \beta$

Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.

The higher the stability factor, the more sensitive is the network to variations in that parameter.

S(ICO)

- Analyze S(ICO) for

– emitter bias configuration

– fixed bias configuration

– Voltage divider configuration

For the emitter bias configuration,

$S(ICO) = (\beta + 1) [1 + RB / RE] / [(\beta + 1) + RB / RE]$ If RB / RE >> $(\beta + 1)$, then

$S(ICO) = (\beta + 1)$

For RB / RE <<1, S(ICO)   1

Thus, emitter bias configuration is quite stable when the ratio RB / RE is as small as possible.

Emitter bias configuration is least stable when RB / RE approaches $(\beta + 1)$.

Fixed bias configuration

$S(I_{CO}) = (\beta + 1) [1 + R_B / R_E] / [(\beta + 1) + R_B / R_E]$

$= (\beta + 1) [R_E + R_B] / [(\beta + 1) R_E + R_B]$

By plugging $R_E = 0$, we get

$S(I_{CO}) = \beta + 1$

This indicates poor stability.

Voltage divider configuration

$S(I_{CO}) = (\beta + 1) [1 + R_B / R_E] / [(\beta + 1) + R_B / R_E]$ Here, replace R_B with R_{th}

$S(I_{CO}) = (\beta + 1) [1 + R_{th} / R_E] / [(\beta + 1) + R_{th} / R_E]$

Thus, voltage divider bias configuration is quite stable when the ratio R_{th} / R_E is as small as possible.

Physical impact

In a fixed bias circuit, IC increases due to increase in IC_0. $[I_C = \beta I_B + (\beta+1) I_{C0}]$

IB is fixed by VCC and RB. Thus level of IC would continue to rise with temperature −

a very unstable situation.

In emitter bias circuit, as IC increases, IE increases, VE increases. Increase in VE reduces IB. IB = [VCC – VBE – VE] / RB. A drop in IB reduces IC.Thus, this configuration is such that there is a reaction to an increase in IC that will tend to oppose the change in bias conditions.

In the DC bias with voltage feedback, as IC increases, voltage across RC increases, thus reducing IB and causing IC to reduce.

The most stable configuration is the voltage – divider network. If the condition βRE

>>10R2, the voltage VB will remain fairly constant for changing levels of IC. VBE =

VB – VE, as IC increases, VE increases, since VB is constant, VBE drops making IB to

fall, which will try to offset the increases level of IC.

S(VBE)

$S(VBE) = \Delta IC / \Delta VBE$

For an emitter bias circuit, $S(VBE) = -\beta / [RB + (\beta + 1)RE]$

If RE =0 in the above equation, we get S(VBE) for a fixed bias circuit as,

$S(VBE) = -\beta / RB$.

For an emitter bias,

$S(VBE) = -\beta / [RB + (\beta + 1)RE]$ can be rewritten as, $S(VBE) = -(\beta/RE) / [RB/RE + (\beta + 1)]$

If $(\beta + 1) >> RB/RE$, then

$S(VBE) = -(\beta/RE) / (\beta + 1)$

$= -1 / RE$

The larger the RE, lower the S(VBE) and more stable is the system. Total effect of all the three parameters on IC can be written as,

$\Delta IC = S(ICO) \Delta ICO + S(VBE) \Delta VBE + S(\beta)\Delta\beta$

General Conclusion:

The ratio RB / RE or Rth / RE should be as small as possible considering all aspects of design.