Unit 2: Transistor Biasing

INTRODUCTION

BJTs amplifier requires a knowledge of both the DC analysis (LARGE-signal) and AC analysis (small signal).

For a DC analysis a transistor is controlled by a number of factors including the range of possible operating points.

Once the desired DC current and voltage levels have been defined, a network must be constructed that will establish the desired operating point.

BJT need to be operate in active region used as amplifier.

The cutoff and saturation region used as a switches.

For the BJTs to be biased in its linear or active operating region the following must be true:

BE junction → forward biased, 0.6 or 0.7V

BC junction → reverse biased

DC bias analysis → assume all capacitors are open cct.

AC bias analysis :

1) Neglecting all of DC sources

2) Assume coupling capacitors are short cct. The effect of these capacitors is to set a lower cut-off frequency for the cct.

3) Inspect the cct (replace BJTs with its small signal model).

4) Solve for voltage and current transfer function and i/o and o/p impedances.

For transistor amplifiers the resulting DC current and voltage establish an operating point that define the region that can be employed for amplification process.

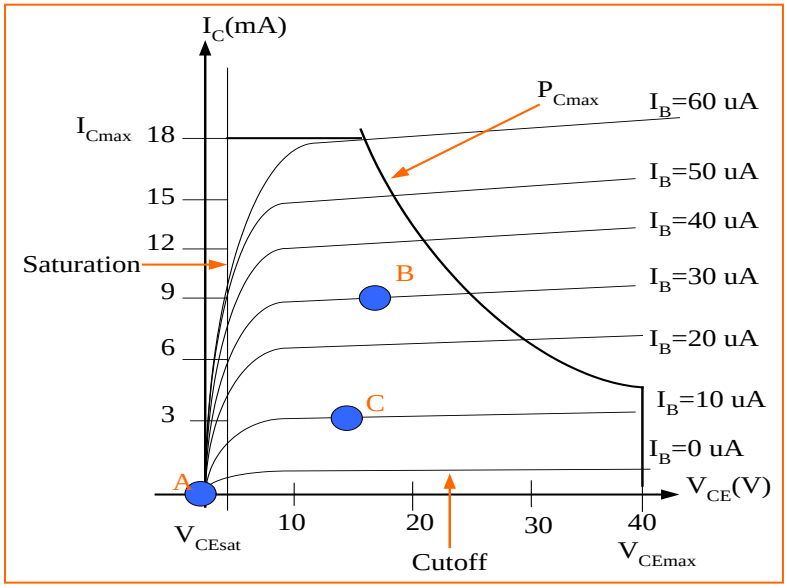
Biasing

Biasing: The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.

Operating Point

The DC input establishes an operating or quiescent point called the Q-point.

Various operating points within the limits of operation of a transistor



Q-point B:

- The best operating point for linear gain and largest possible voltage and current
- It is a desired condition for a small signal analysis

Q-point A:

- I=0A, V=0V
- Not suitable for transistor to operate

Q-point C:

- Concern on nonlinearities due to I_B
- curves is rapidly changes in this region.

The Three States of Operation

• Active or Linear Region Operation

Base–Emitter junction is forward biased

Base–Collector junction is reverse biased

• Cutoff Region Operation

Base–Emitter junction is reverse biased

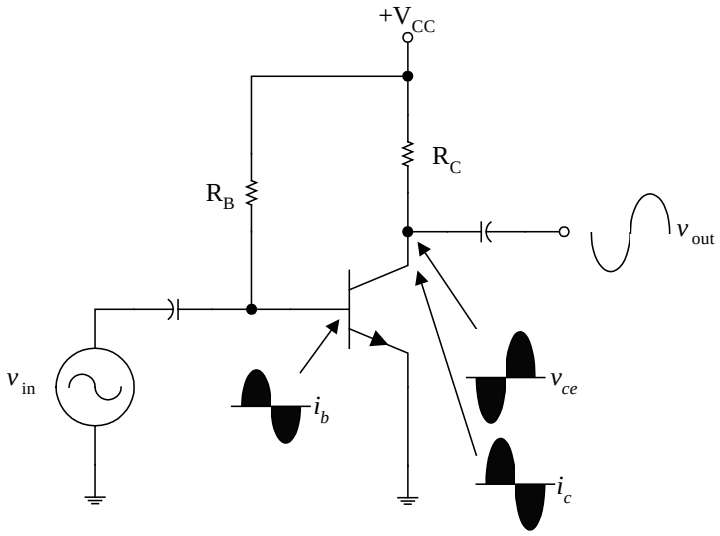
• Saturation Region Operation

Base–Emitter junction is forward biased

Base–Collector junction is forward biased

DC Biasing Circuits

The **ac** operation of an amplifier depends on the initial **dc** values of I_B, I_C, and V_{CE}. By varying I_B around an initial dc value, I_C and V_{CE} are made to vary around their initial dc values. **DC** biasing is a static operation since it deals with setting a **fixed (steady)** level of current (through the device) with a desired fixed voltage drop across the device.

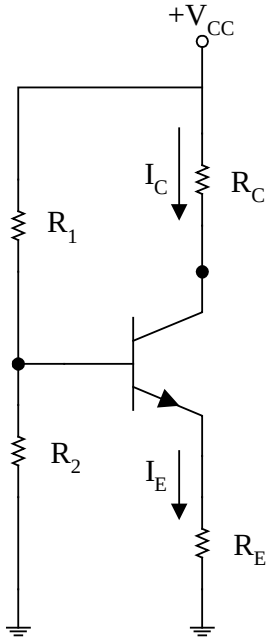


Purpose of the DC biasing circuit To turn the device “ON” . To place it in operation in the region of its characteristic where the device operates most linearly, i.e. to set up the initial dc values of IB, IC, and VCE

Types

- Fixed-bias circuit
- Emitter-stabilized bias circuit
- Collector-emitter loop
- Voltage divider bias circuit
- DC bias with voltage feedback

Graphical DC Bias Analysis



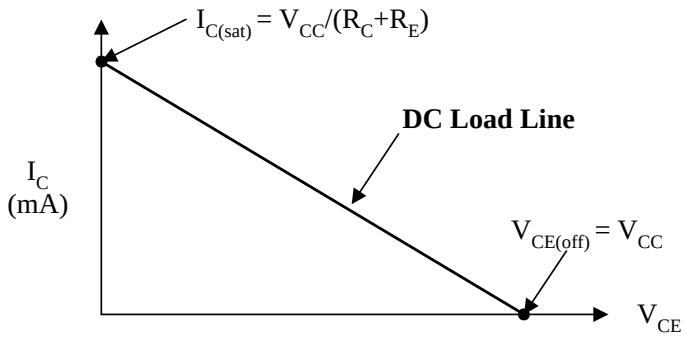
$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\text{for } I_C \approx I_E$$

$$I_C = \frac{-1}{R_C + R_E} V_{CE} + \frac{V_{CC}}{R_C + R_E}$$

Point - slope form of straight line equation :

$$y = mx + c$$



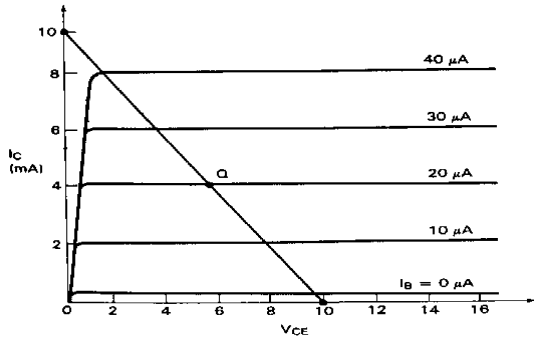
DC Load Line

The straight line is know as the **DC load line**

Its significance is that regardless of the behavior of the transistor, the collector current I_C and the collector-emitter voltage V_{CE} must always lie on the load line, depends ONLY on the V_{CC}, R_C and R_E (i.e. The dc load line is a graph that **represents all the possible combinations of I_C and V_{CE} for a given amplifier**. For every possible value of I_C, and amplifier will have a corresponding value of V_{CE}.)

It must be true at the same time as the transistor characteristic. Solve two condition using simultaneous equation

→ graphically → **Q-point !!**



Q-Point (Static Operation Point)

When a transistor does not have an **ac input**, it will have **specific dc values** of I_C and V_{CE}.

These values correspond to a specific point on the **dc load line**. This point is called the ***Q-point***.

The letter ***Q*** corresponds to the word (Latent) **quiescent**, meaning **at rest**.

A quiescent amplifier is one that has no ac signal applied and therefore has constant dc values of I_C and V_{CE}.

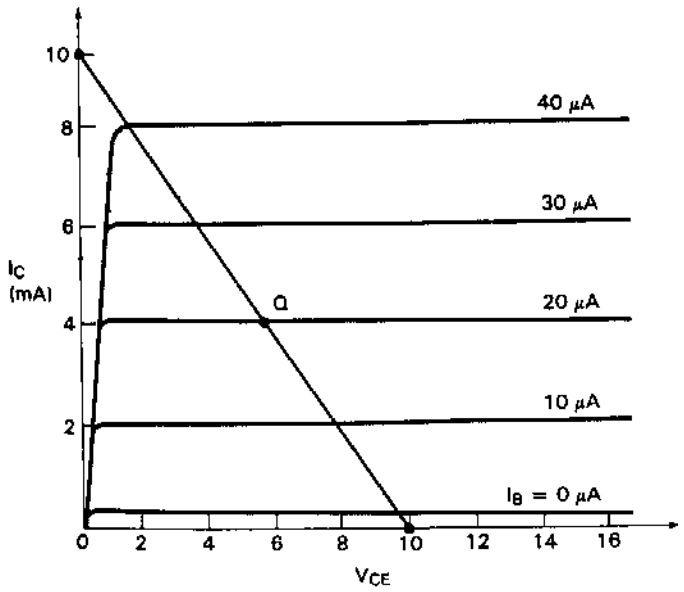
The intersection of the dc bias value of I_B with the dc load line determines the *Q*-point.

It is desirable to have the *Q*-point centered on the load line.

Why?

When a circuit is designed to have a centered *Q*-point, the amplifier is said to be midpoint biased.

Midpoint biasing allows optimum ac operation of the amplifier.



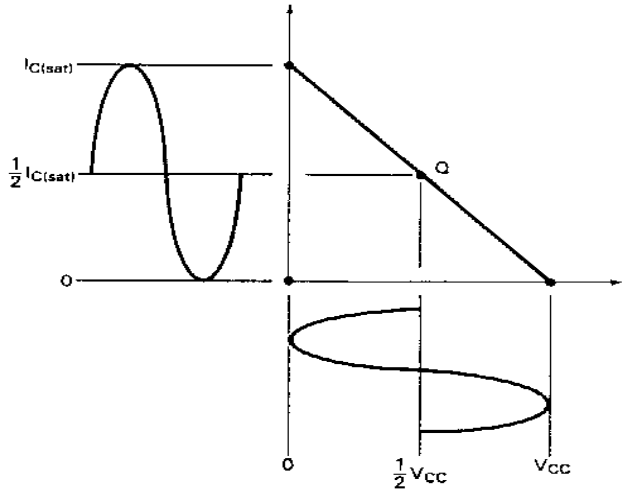
DC Biasing + AC signal

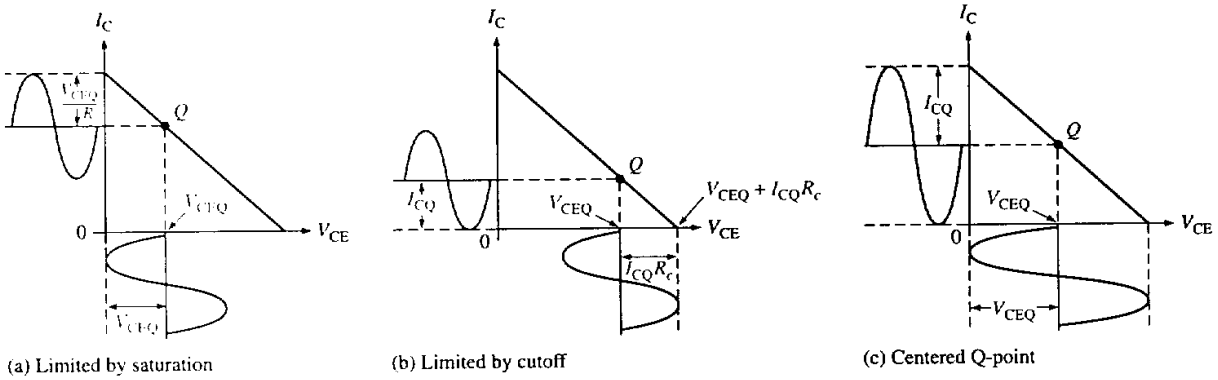
When an **ac signal** is applied to the base of the transistor, I_C and V_{CE} will both vary around their *Q*-point values.

When the *Q*-point is **centered**, I_C and V_{CE} can both make the **maximum** possible transitions above and below their initial dc values.

When the *Q*-point is **above** the center on the load line, the input signal may cause the transistor to saturate. When this happens, a part of the output signal will be ***clipped*** off.

When the *Q*-point is **below** midpoint on the load line, the input signal may cause the transistor to cutoff. This can also cause a portion of the output signal to be clipped.



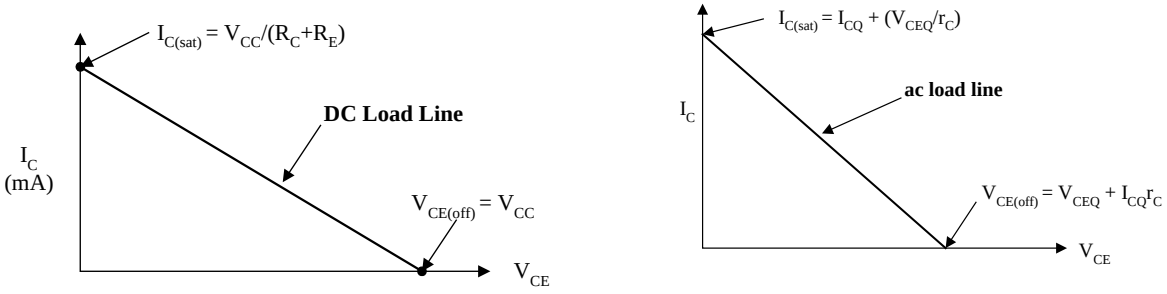


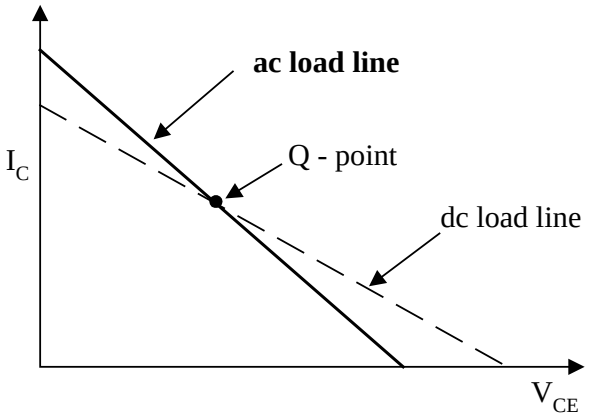
(a) Limited by saturation (b) Limited by cutoff (c) Centered Q-point

AC Load Line

- The ac load line of a given amplifier will **not follow** the plot of the dc load line.

This is due to the dc load of an amplifier is different from the ac load





What does the ac load line tell you?

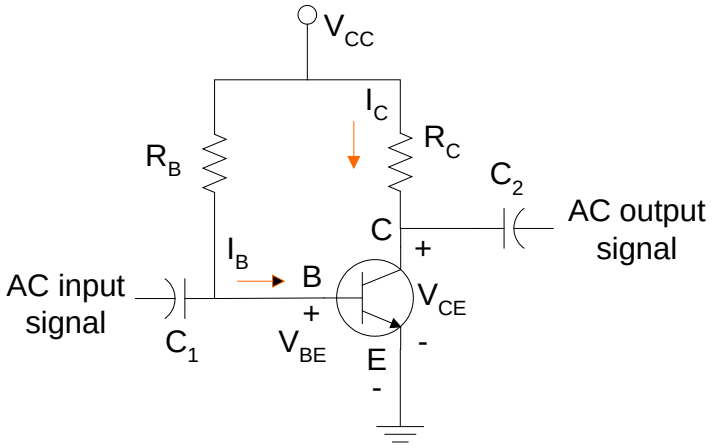
The ac load line is used to tell you the maximum possible output voltage swing for a given common-emitter amplifier.

In other words, the ac load line will tell you the maximum possible peak-to-peak output voltage (V_{pp}) from a given amplifier.

This maximum V_{pp} is referred to as the **compliance** of the amplifier.

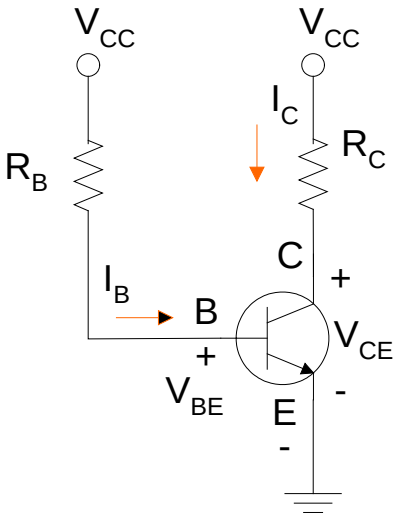
(AC Saturation Current $I_{c(sat)}$, AC Cutoff Voltage $V_{CE(off)}$)

Fixed Bias



C_1,C_2 = coupling capacitors

AC ANALYSIS

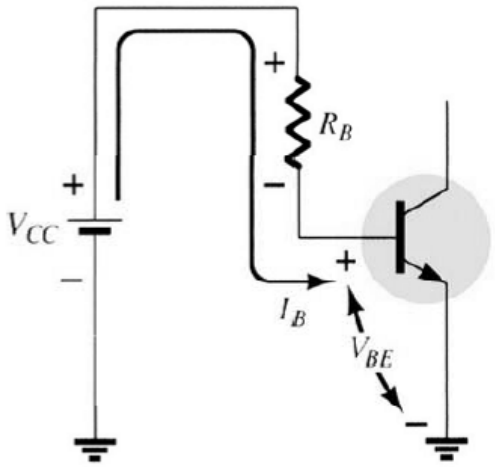


DC ANALYSIS

The Base-Emitter Loop

From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$



Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

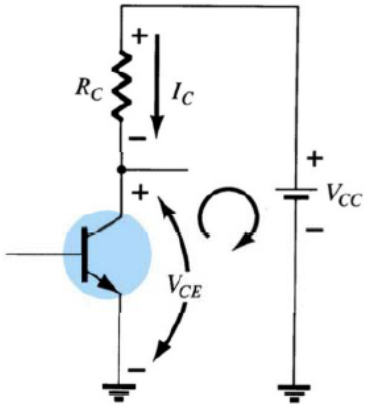
Collector-Emitter Loop

Collector current:

$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$



Saturation

When the transistor is operating in saturation, current through the transistor is at its *maximum* possible value.

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

$$V_{CE} \cong 0\,V$$

Load Line Analysis

The end points of the load line are:

I_{Csat}

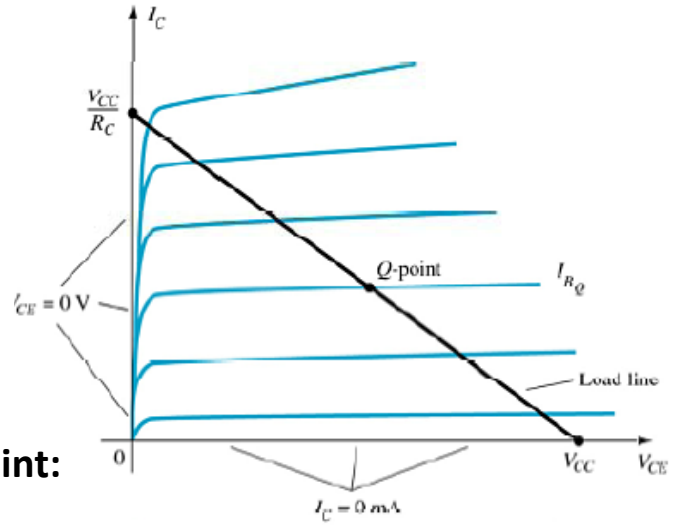
$I_C = V_{CC} / R_C$

$V_{CE} = 0$ V

$V_{CEcutoff}$

$V_{CE} = V_{CC}$

$I_C = 0$ mA

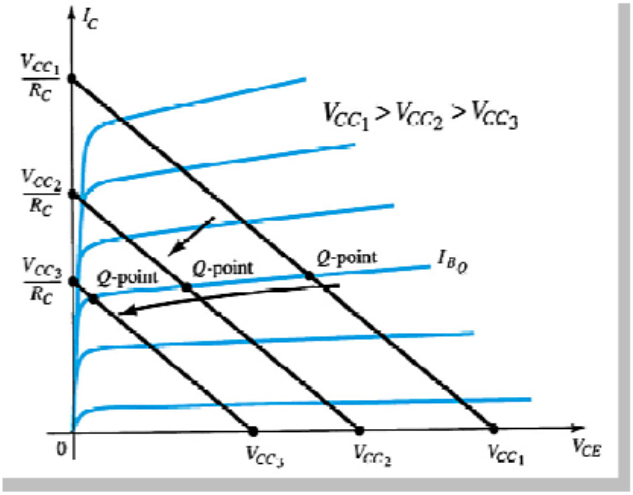


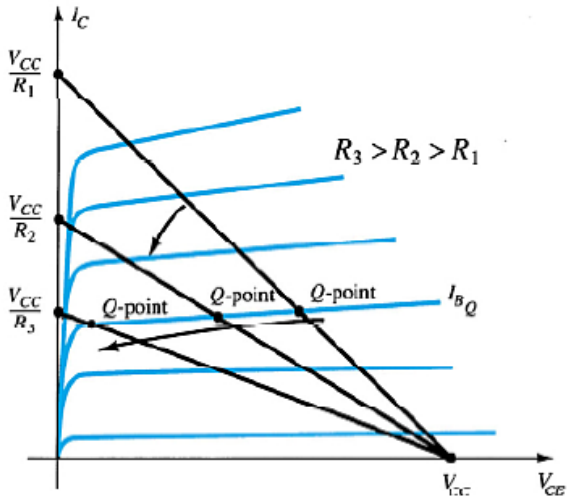
The *Q*-point is the operating point:

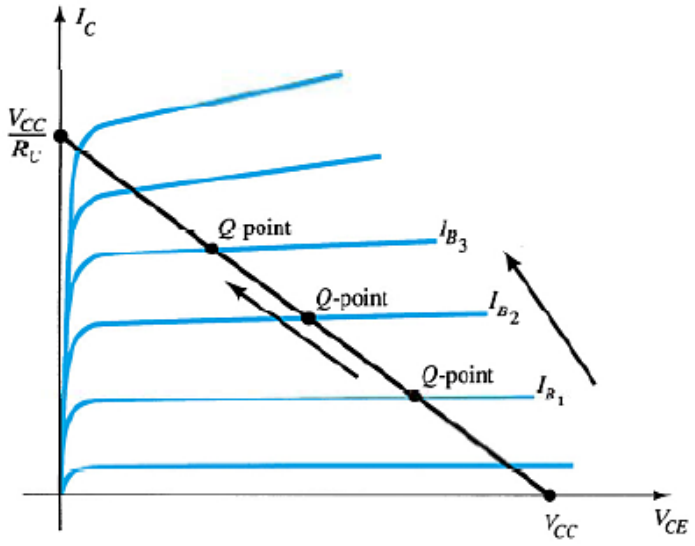
- where the value of RB sets the value of IB
- sets the V and I

that values of V_{CE} I_C

Circuit values affect the Q point

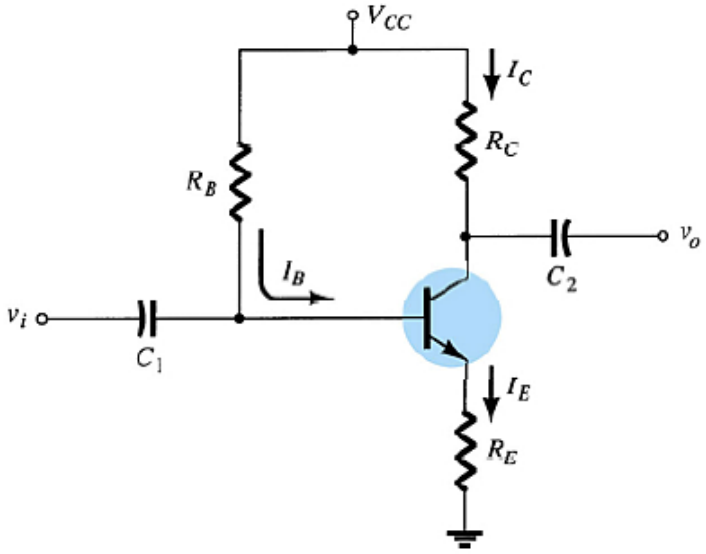






Emitter-Stabilized Bias Circuit

Adding a resistor (RE) to the emitter circuit stabilizes the bias circuit.



Base-Emitter Loop

From Kirchhoff's voltage law:

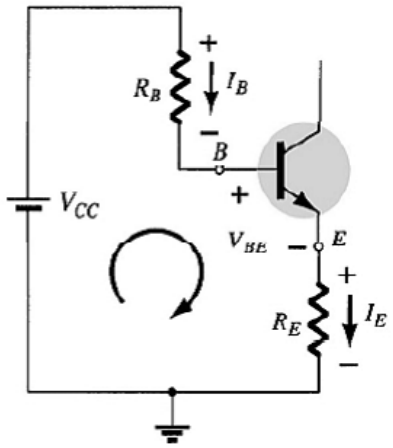
$$+V_{CC} - I_E R_E - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$:

$$V_{CC} - I_B R_B - (\beta + 1) I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$



Collector Emitter Loop

From Kirchhoff's voltage law:

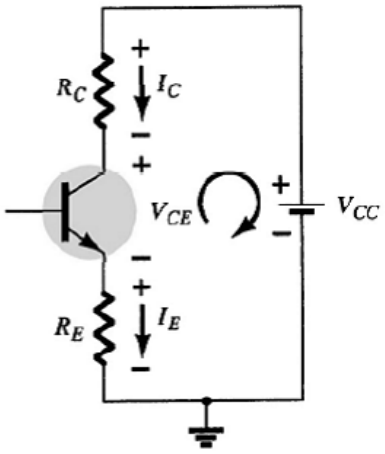
$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \cong I_C$:

$$V_{CE} = V_{CC} \quad I_C (R_C + R_E)$$

Also:

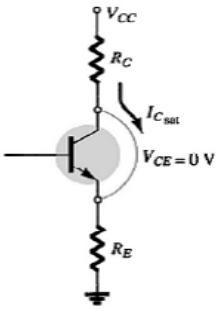
$$V_E = I_E R_E$$
$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$
$$V_B = V_{CC} - I_R R_B = V_{BE} + V_E$$

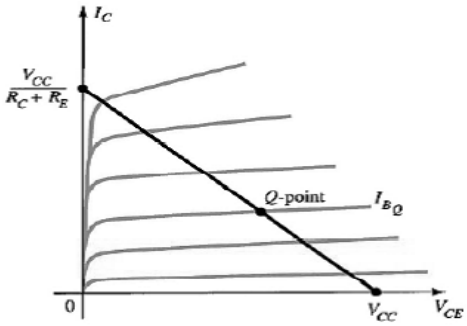


Improved Biased Stability

Stability refers to a circuit condition in which the currents and voltages will remain fairly constant over a wide range of temperatures and transistor Beta (β) values. Adding RE to the emitter improves the stability of a transistor.

Saturation Level





The endpoints can be determined from the load line.

$\mathbf{V_{CEcutoff}}$:

$$\mathbf{V_{CE} = V_{CC}}$$
$$\mathbf{I_C = 0\ mA}$$

$\mathbf{I_{Csat}}$:

$$\mathbf{V_{CE} = 0\ V}$$
$$\mathbf{I_C = \frac{V_{CC}}{R_C + R_E}}$$

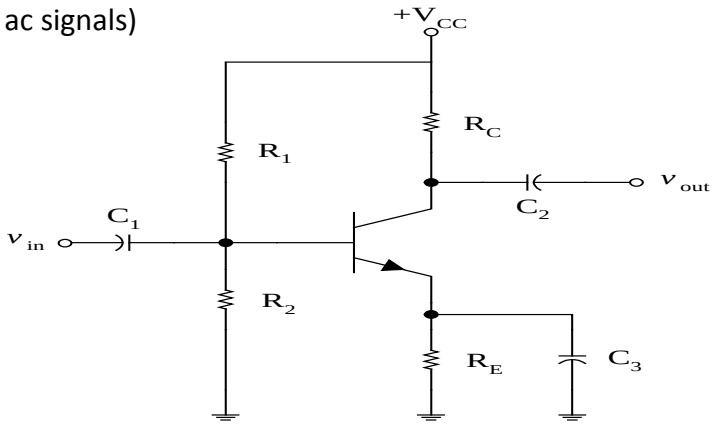
Voltage-Divider Bias

The voltage – divider (or potentiometer) bias circuit is by far the most commonly used.

RB1, RB2 -> voltage-divider to set the value of VB , IB

C3 -> to short circuit ac signals to ground, while not effect the DC operating (or biasing) of a circuit

(RE stabilizes the ac signals)



Approximate Analysis

Where $I_B << I_1$ and $I_1 \cong I_2$:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10R_2$:

$$I_E - \frac{V_E}{R_E}$$

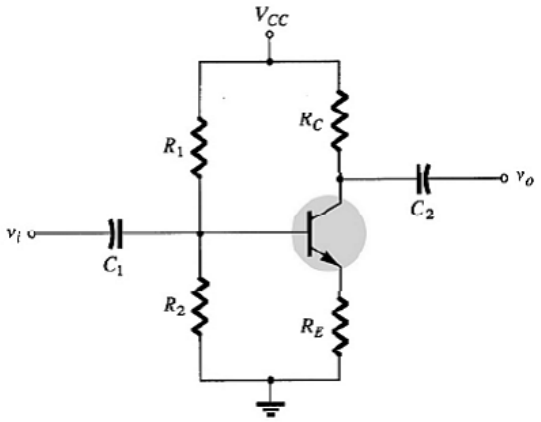
$$V_E = V_B - V_{BE}$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



Voltage Divider Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$

$$I_C = 0mA$$

Saturation:

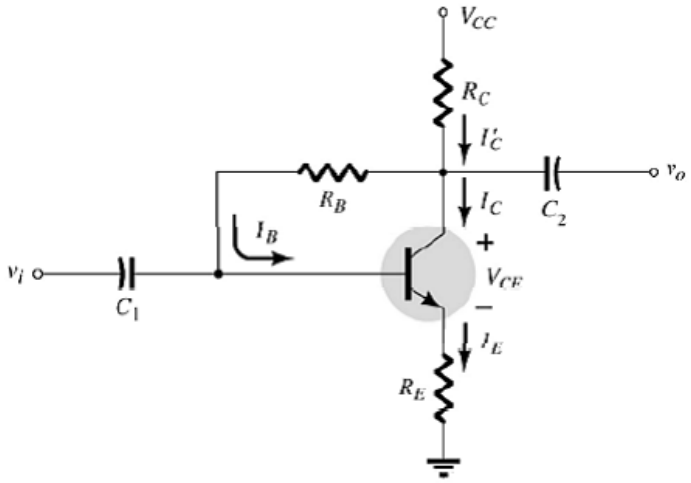
$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0V$$

DC Bias with Voltage Feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

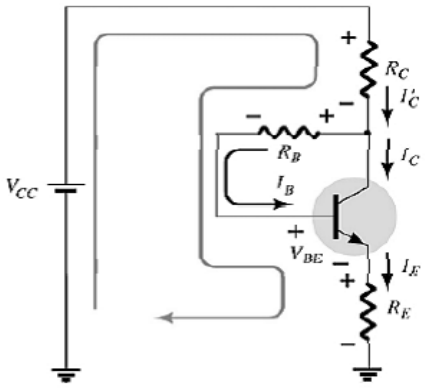
In this bias circuit the Q-point is only slightly dependent on the transistor beta, β.



Base-Emitter Loop

From Kirchhoff's voltage law:

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$



Where $I_B << I_C$:

$$I'_C = I_C + I_B \cong I_C$$

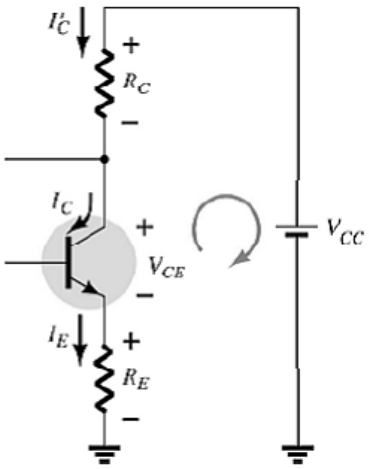
Knowing $I_C = \beta I_B$ and $I_E \cong I_C$, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

Collector Emitter Loop



Applying Kirchoff's voltage law:

$$I_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_C = \beta I_B$:

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

Solving for V_{CE}:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Base Emitter Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

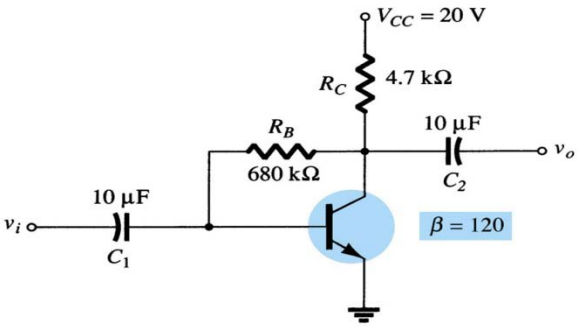
Cutoff:

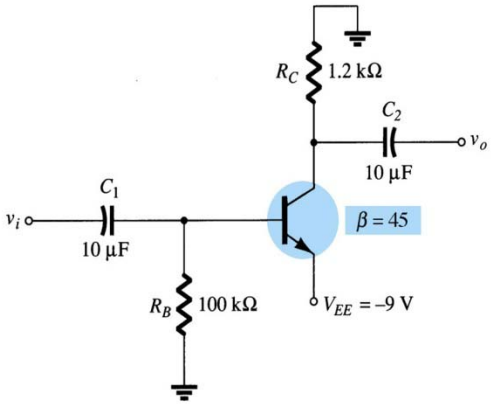
$$V_{CE} = V_{CC}$$
$$I_C = 0\,\text{mA}$$

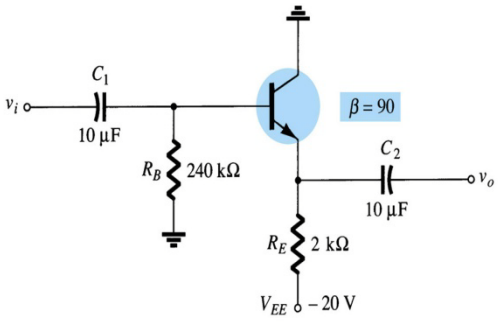
Saturation:

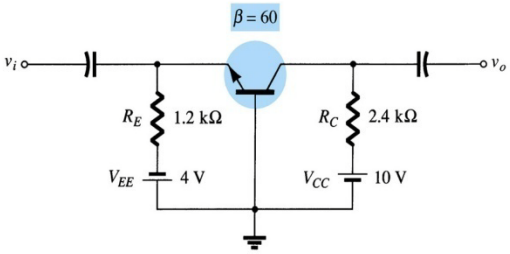
$$I_C = \frac{V_{CC}}{R_C + R_E}$$
$$V_{CE} = 0\,\text{V}$$

Miscellaneous configuration









Transistor Switching Networks

Transistor works as an inverter in computer circuits.

Operating point switch from cut-off to saturation along the load line for proper inversion.

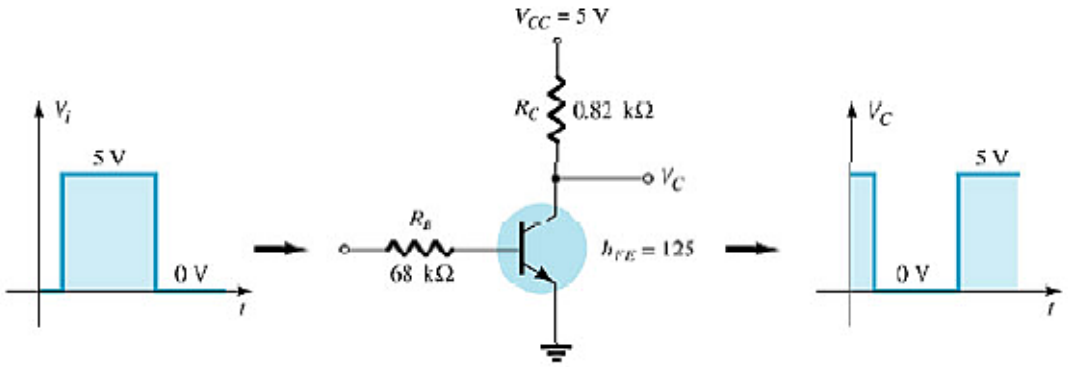
In order to understand, we assume that;

IC=ICEO=0mA

VCE=Vsat=0V

One must understand the transistor graph output and load-line analysis to describe and discuss about the transistor switching networks.

Transistors with only the DC source applied can be used as electronic switches.



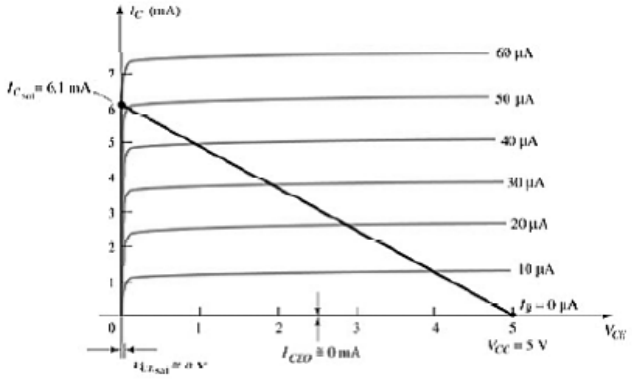
Switching Circuit Calculations

Saturation current:

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

To ensure saturation:

$$I_B > \frac{I_{Csat}}{\beta_{dc}}$$



Emitter-collector resistance at saturation and cutoff:

$$R_{sat} = \frac{V_{CEsat}}{I_{Csat}}$$

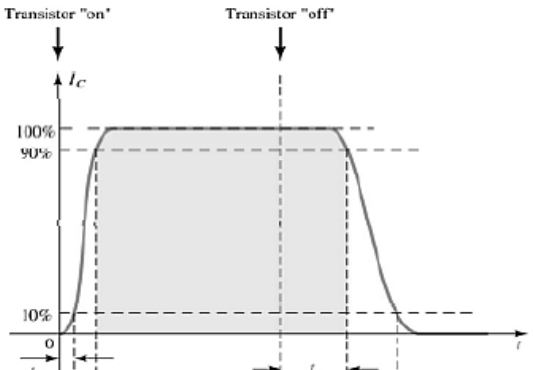
$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}}$$

Switching Time

Transistor switching times:

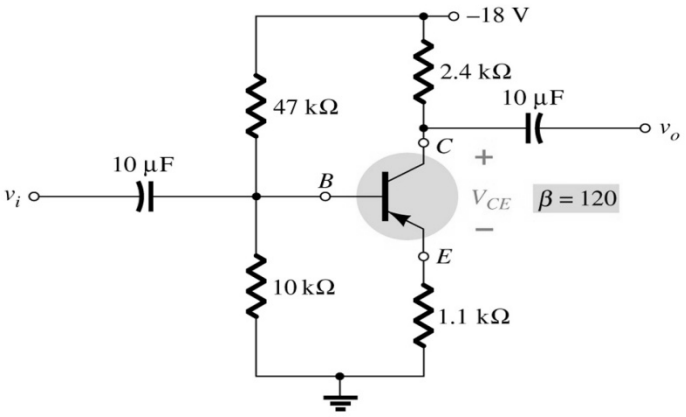
$$t_{on} = t_r + t_d$$

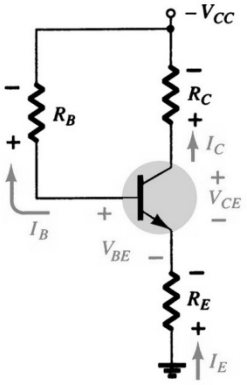
$$t_{off} = t_s + t_f$$



PNP Transistors

The analysis for *pnp* transistor biasing circuits is the same as that for *npn* transistor circuits. The only difference is that the currents are flowing in the opposite direction.

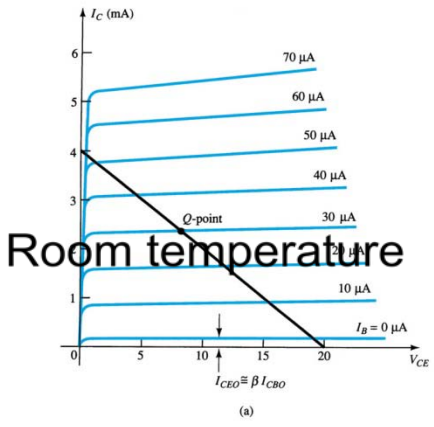


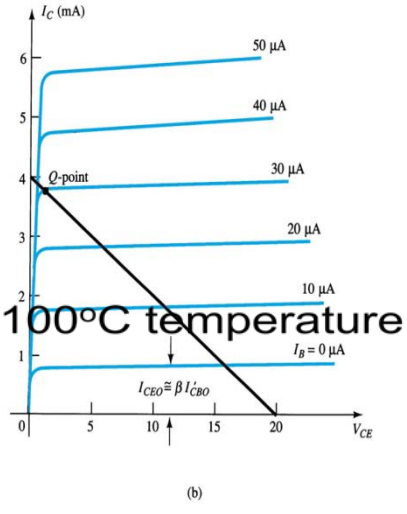


Bias stabilization

- Stability of a system is a measure of the sensitivity of a network to variation in its parameter.
  - β increases with increase in temperature
  - V_{BE} decreases 7.5mV every degree celcius
  - I_{CO} doubles every 10 ^{o}C increase in temperature

Effect of non-stability circuit/system





We'll find that β increase after 100^{O}C, base current is same but not suitable to use due it is very near to the saturation region.

Stability factors

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

$S(I_{CO})$

Emitter bias configuration

$$S(I_{CO}) = (\beta+1)\frac{1+(\frac{R_B}{R_E})}{(\beta+1)+(\frac{R_B}{R_E})}$$

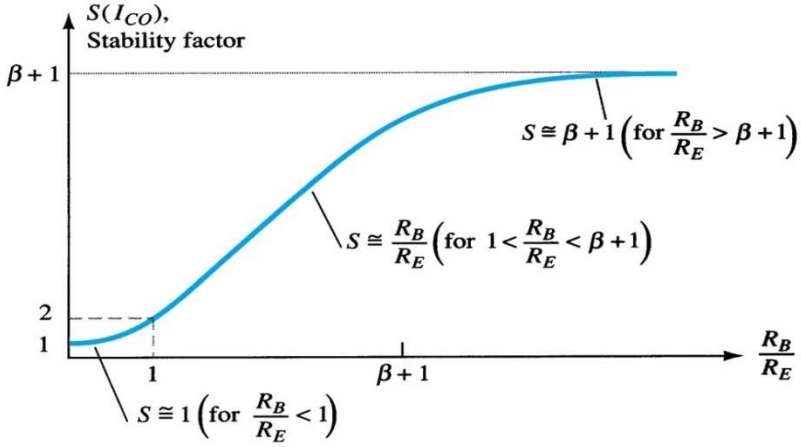
If $R_B/R_E >> (\beta+1)$, it will reduce to

$S(I_{CO}) = (\beta+1)$

If $R_B/R_E << (\beta+1)$, it will reduce to

$S(I_{CO}) = 1$

For ranges of R_B/R_E from 1 to $\beta+1$, stability factor will be, $S(I_{CO}) \cong R_B/R_E$



- Fixed bias configuration

$$S(I_{CO}) = (\beta + 1)\frac{1 + (\frac{R_B}{R_E})}{(\beta + 1) + (\frac{R_B}{R_E})}$$

If multiplying above equation with R_E for the numerator and denumerator, and assume $R_E = 0\Omega$ we'll obtain,

$S(I_{CO}) = (\beta + 1)$....so it's not stable and reach the maximum value

- Voltage divider bias configuration

$$S(I_{CO}) = (\beta + 1)\frac{1 + (\frac{R_{Th}}{R_E})}{(\beta + 1) + (\frac{R_{Th}}{R_E})}$$

This is same to the emitter - bias configuration characteristic, but differs only because analyze using Thevenin rule.

- Feedback bias configuration

$$S(I_{CO}) = (\beta + 1)\frac{1 + (\frac{R_B}{R_C})}{(\beta + 1) + (\frac{R_B}{R_C})}$$

Where $R_E = 0\Omega$

- Physical impact

Fixed bias configuration ; $I_C = \beta I_B + (\beta+1)I_{CO}$...$I_C$ increase but I_B maintain, so it's not stable

Emitter bias configuration ; Increase I_C will increase I_{CO}. It affect V_E since $V_E=I_ER_E=I_CR_E$. In turn, the output loop will inform that I_B will decrease if V_E is increase, thus affect to reduce the collector current.

Feedback bias configuration ; same as result of emitter bias configuration where I_B will decrease if I_C increase. (I_C proportional to V_{RC})

Voltage divider bias configuration ; Most stable where as long as $10R_2 >> \beta R_E$, V_B remain constant for any changing in I_C.

$S(V_{BE})$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

$$= \frac{-\beta}{R_B + (\beta+1)R_E}$$

$$= -\frac{\beta}{R_B} \text{.....(if } R_E = 0\Omega)$$

or

$$= \frac{\frac{-\beta}{R_E}}{\frac{R_B}{R_E} + (\beta+1)}$$

$$= -\frac{1}{R_E} \text{.....(if } \beta+1 >> R_B/R_E)$$

$S(\beta)$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta}$$

$$= I_C \frac{I_C + (1+\frac{R_B}{R_E})}{\beta_1(1+\beta_2+\frac{R_B}{R_E})}$$

Example 1:

Determine the following for the fixed bias configuration of Fig 5.3.

a) I_{BQ} and I_{CQ} b) V_{CEQ} c) V_B and V_C d) V_{BC}

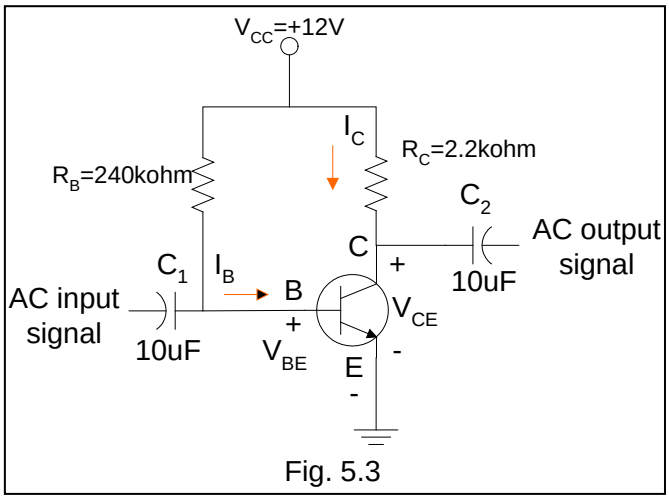


Fig. 5.3

Solution:

$$a)\ I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{12 - 0.7}{240k} = \underline{\underline{47.08uA}}$$

$$I_{CQ} = \beta I_{BQ} = (50)(47.08u) = \underline{\underline{2.34\ mA}}$$

$$b)\ V_{CEQ} = V_{CC} - I_C R_C$$

$$= 12 - (2.35\text{m})(2.2k)$$

$$= \underline{\underline{6.83V}}$$

$$c)\ V_{BE} = V_B = \underline{\underline{0.7\ \text{V}}}$$

$$V_{CE} = V_{CEQ} = V_C = \underline{\underline{6.83\ \text{V}}}$$

$$d)\ V_{BC} = V_B - V_C = 0.7 - 6.83 = \underline{\underline{-6.13\text{V}}}$$

- ve sign indicates that BC - junction is reverse biased.

Determine the following for the fixed bias configuration of Fig 5.4.

a) I_{BQ} and I_{CQ} b) V_{CEQ} c) V_B d)V_C e) V_E

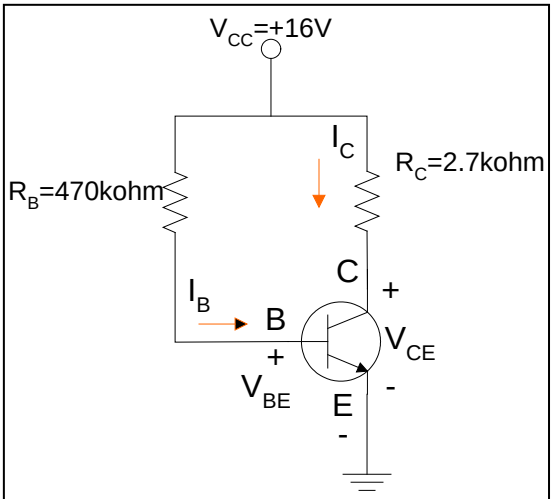


Fig. 5.4

$$a)\ I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{16 - 0.7}{470k} = \underline{\underline{32.55uA}}$$

$$I_{CQ} = \beta I_{BQ} = (90)(32.55u) = \underline{\underline{2.93\,mA}}$$

$$b)\ V_{CEQ} = V_{CC} - I_C R_C$$

$$= 16 - (2.93\text{m})(2.7k)$$

$$= \underline{\underline{8.17V}}$$

$$c)\ V_{BE} = V_B = \underline{\underline{0.7\ V}}$$

$$d) V_{CE} = V_{CEQ} = V_C = \underline{\underline{8.17\ V}}$$

$$e) V_E = \underline{\underline{0V}}$$

Example 6:

Determine the value of Q-point for Fig. 5.11. Also find the new value of Q-point if β change to 150.

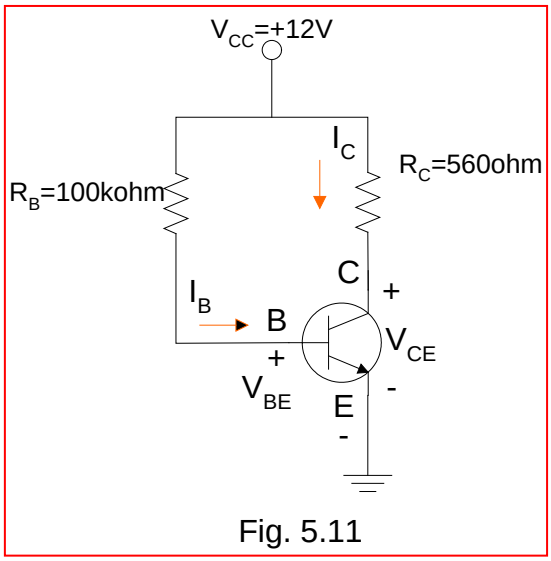


Fig. 5.11

$$\text{Step 1:}$$
$$\beta = 100,$$
$$I_B = \frac{12 - 0.7}{100k} = 113\ \mu A$$
$$I_C = \beta I_B = (100)(113\mu) = 11.3\ mA$$

$$\text{Step 2:}$$
$$V_{CE} = V_{CC} - I_C R_C$$
$$= 12 - (11.3m)(560)$$
$$= 5.67V \Rightarrow \underline{\underline{Q - point(5.67V, 11.3mA)}}$$

$$\text{Step 3: new } \beta = 150,$$
$$I_B = \frac{12 - 0.7}{100k} = 113\ \mu A \Rightarrow \text{the value is same,}$$
$$I_C = \beta I_B = (150)(113\mu) = 16.95\ mA$$

$$\text{Step 4:}$$
$$V_{CE} = V_{CC} - I_C R_C$$
$$12 - (16.95m)(560)$$
$$2.51V \Rightarrow \underline{\underline{\text{New Q - point } (2.51\text{ V}, 16.95mA)}}$$

The change of β cause the big change of

Q-point value. This shows that fixed biased configuration is NOT stable