10ES32 - Analog Electronic Circuits

Assignment-II

Note: i) Write the assignment in a A4 size paper
iii) Mention your USN, name and section on the top right corner of first page
iii) Assume the missing data suitably
iv) Submit the assignment on or before 11.00 AM, Monday, 7/10/2013

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1. Explain transistor switching network.
2. Derive the expressions for S, S', and S'' for i) Emitter Bias, ii) Voltage Divider Bias, and iii) Collector Feedback Bias.
3. Design a voltage divider bias circuit to get the Q point I_{CQ} = 3mA and V_{CEQ} = 7V.
4. Design a emitter bias circuit to get the Q point I_{CQ} = 2.1mA and V_{CEQ} = 5V.
5. Design a collector feedback bias circuit to get the Q point I_{CQ} = 1mA and V_{CEQ} = 6V.
6. For a voltage divider bias circuit, R_1= 62 KΩ, R_2= 9.1 KΩ, R_E= 680 Ω, R_C=3.9 KΩ, V_{cc}=16V, β=80, calculate S and S'.
7. Determine the stability factor S(β) and the change in Ic from 25° C to 100° C for the transistor with β (25° C) = 50 and β (100° C)= 100 for the following bias arrangement.
   a) Fixed bias with R_B= 330 KΩ
   b) Emitter bias with R_B/R_E=5
   c) Voltage divider bias with R_{TH}/R_E=1.5

   Also calculate I_{CQ} at the 100° C in each case if I_{CQ} at 25° C is 3 mA
8. What is Barkhausen criterion? Explain how oscillations start in an oscillator.
9. Design a transistor Hartley oscillator to generate a frequency of 175KHz. Consider H_{fe}=45.
10. Explain the merits and demerits of RC phase shift oscillator
11. A quartz crystal has L = 0.12H, C = 0.04 pF, C_M = 1pF and R = 9.2 kΩ. Find i) Series resonant frequency, ii) Parallel resonant frequency and iii) Quality factor.